MBM-530NS
User’ s Manual

Copyright Notice

Trademarks

Products and corporate names appearing in this manual may or may not be registered trademarks or copyrights of their respective companies, and are used only for identification or explanation and to the owners' benefit, without intent to infringe.

- Intel and Celeron are registered trademarks of Intel Corporation.
- Windows and MS-DOS are registered trademarks of Microsoft Corporation.
- Award is a registered trademark of Award Software International, Inc.
- IBM and PS/2 are trademarks of International Business Machines.
- VIA is a registered trademark of VIA Technologies, Inc.
- NSTL is the trademark of National Software Test Lab.

Liability

This User Guide is composed to assist system manufacturers and end users in setting the Single Board Computer (SBS). FIC provides this guide "AS IS" without warranty of any kind, either express or implied, including but not limited to the implied warranties or conditions of merchantability or fitness for a particular purpose. In no events shall FIC, its directors, officers, employees or agents be liable for any indirect, special, incidental or consequential damages (including damages for loss of profits, loss of business, loss of use or data, interruption of business and the like), even if FIC has been advised of the possibility of such damages arising from any defects or errors in this manual or product.

Specifications and information contained in this manual are furnished for informational use only, and are subject to change at any time without notice, and should not be construed as a commitment by FIC. FIC reserves the right to make revisions to this publication without the obligation to notify any persons or entities of any changes. FIC assumes no responsibility or liability for any errors or inaccuracies that may appear in this manual, including the products and software described in it.

Others

Please inform your dealer immediately should there be any incorrect, missing or damaged parts.

Please retain the carton, including the original packing materials. Repack the product in the original way in case there is a need to return it to the manufacturer for repairing.

Products warranty or service will not be extended if: (1) the product is repaired, modified or altered, unless such repair, modification or alternation is authorized in writing by FIC; or (2) the serial number of the product is defaced or missing.

Safety Precautions

- Follow the messages hereinafter to protect your systems from damage on all occasion.
- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strop).
- Stay safe from the electric shock. Don' t touch any components of this card when the card is on. Always switch off power when the system is not in use.
- Disconnect power when changing any hardware device; For instance, when you connect a jumper or install any cards, a surge of power may damage the electronic components or the whole system.

Product Name:	**MBM-530NS**
Manual Version:	**English, 1st edition (E0301-R01)**
Document Part No.:	**C251-530NS-FIC**
Release Date:	**March 2001**
Printed in Taiwan	

Formosa Industrial Computing, Inc.

Sales:

Address: 8F-6, No. 351, Sec. 2, Chung Shan Rd., Chung Ho City, Taipei,

Taiwan 235

Telephone: +886-2-3234-7000

Fax: +886-2-2226-9623

E-mail: ipcsales@nfic.com.tw

Technical Support:

Address: 8F-6, No. 351, Sec. 2, Chung Shan Rd., Chung Ho City, Taipei,

Taiwan 235

Telephone: +886-2-3234-7000

Fax: +886-2-2226-9623

E-mail: ipcservice@nfic.com.tw

Formosa USA, Inc.:

Address: 21540 Praire Street, Unit A, Chatsworth, CA91311, U.S.A.

Telephone: +1-818-407-4965

Fax: +1-818-407-4966

E-mail: formosausa@aol.com

Beijing Branch Office:

Telephone: +86-10-6252-0215

Fax: +86-10-6252-0219

E-mail: kunga@nfic.com.tw

Shanghai Branch Office:

Telephone: +86-10-6252-0215

Fax: +86-10-6252-0215

E-mail: albertyu@nfic.com.tw

Shenzhen Branch Office:

Telephone: +86-755-379-1219

Fax: +86-755-379-1100

E-mail: matt@nfic.com.tw

Table of Contents

0. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

0.1 Introduction

The MBM-530NS is new generation half-size CPU board. This card offers much greater performance than the older cards, such as support for four RS-232C ports and one 168-pin DIMM socket for up to 128MB of extended memory SDRAM.

The unit also comes with a programmable watchdog timer and other standard interfaces. The CPU board is excellent for embedded systems, MMI' s, Workstations, medical applications or POS/POI systems.

The on-board VGA offers the most exciting possibilities yet to the industry. The on-board VGA/LCD controller brings about a whole new dimension in industrial computing. No longer do you have to worry about adding an extra card to your system.

0.2 Packing List

Some accessories are included with the system. Before you begin installing your MBM-530NS board, take a moment to make sure that the following items have been included inside the MBM-530NS package.

- MBM-530NS all-in-one single CPU board
- Hard disk drive interface cable
- Parallel port interface cable
- Floppy interface cable
- PS/2 mouse / keyboard adapter cable
- USB cable
- Audio adapter cable
- COM port cable
- User' s Manual
- Software utility driver
- LCD cable (optional)
- IR cable (optional)
- TTL I/O cable (optional)

0.3 Features

The system provides a number of special features that enhance its reliability, ensure its long-term availability, and improve its expansion capabilities, as well as its hardware structure.

- NS GX1-300 MHz CPU
- On chip UMA-system VGA (On-board CRT and 18 bit TFT-LCD panel display)
- Supports IDE hard disk drives
- Supports floppy disk drives
- Supports 1 bi-directional parallel port
- Supports 2 USB port
- Supports 16-bit PnP sound system
- 100/10 BaseT Ethernet with RJ-45 connector
- PC/AT compatible keyboard
- Programmable watchdog timer
- AWARD Flash BIOS
- Multi-layer PCB for noise reduction
- 2 COM ports: 1 of the 2 is switchable to RS-485/ RS-422/RS-232
- Supports IrDA compatible transmissions
- Dimensions: 140mm X 145mm

1. SYSTEM CONTROLLER

This chapter describes the main structure of the MBM-530NS CPU board.
The following topics are covered:

- Microprocessors
- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Serial Port
- Parallel Port

1.1 Microprocessor

The MBM-530NS uses the NS GX1-300 CPU (or other GX1 CPUs); it is an advanced 64-bit x86 compatible processor offering high performance, fully accelerated 2D graphics, a 64-synchronous DRAM controller and a PCI bus controller, all on a single chip. This latest generation of the MediaGX processor enables a new class of premium performance notebook/desktop, and IPC computer designs.
The MediaGX MMX enhanced processor companion chips provide advanced video and audio functions and permit direct interface to memory. This high-performance 64-bit processor is x86 instruction set compatible and supports MMX technology.

This processor is the latest member of the NS MediaGX family, offering high performance, fully accelerated 2D graphics, synchronous memory interface and a PCI bus controller, all on a single chip. As described in separate manuals, the Cx5530A I/O Companion chips fully enable the features of the MediaGX processor with MMX support. These features include full VGA and VESA video, 16-bit stereo sound, IDE interface, ISA interface, SMM power management, and AT compatibility logic. In addition, the newer CX5530A provides an Ultra DMA/33 interface, MPEG2 assist, and is AC97 Version 2.0 audio compliant.

In addition to the advanced CPU features, the MediaGX processor integrates a host of functions, which are typically implemented with external components. A full-function graphics accelerator provides pixel processing and rendering functions.

The NS MediaGX MMX-Enhanced Processor represents a new generation of x86-compatible 64-bit microprocessors with sixth-generation features. The decoupled load/store unit (within the memory management unit) allows multiple instructions in a single clock cycle. Other features include single-cycle execution, single-cycle instruction decode, 16KB write-back cache, and clock rates up to 300MHz. These features are possible by the use of advanced-process technologies and super pipelining.

1.2 DMA Controller

The equivalent of two 8237A DMA controllers are implemented on the MBM-530NS board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The Following is the system information for the DMA channels:

Slave with four 8-bit channels	**Master with three 16-bit channels**
DMA Controller 1	**DMA Controller 2**
Channel 0: Spare	Channel 4(0): Cascade for controller 1
Channel 1: IBM SDLC	Channel 5(1): Spare
Channel 2: Diskette adapter	Channel 6(2): Spare
Channel 3: Spare	Channel 7(3): Spare

1.3 Keyboard Controller

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

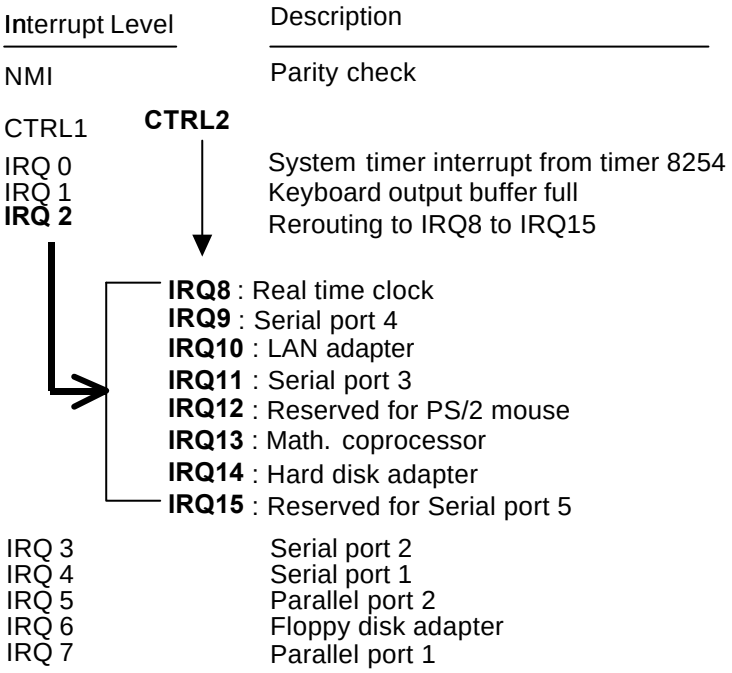
Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in a series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interruption may be used for both send and receive routines.

1.4 Interrupt Controller

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the MBM-530NS board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute. These two controllers are cascaded with the second controller representing IRQ8 to IRQ15, which is rerouted through IRQ2 on the first controller.

The following is the system information of interrupts levels:



1.4.1 I/O Port Address Map

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	NS CX5530A
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
218-21A	EMS register 1
278-27F	Parallel printer port 2 (LPT 2)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
300-31F	Prototype card/streaming type adapter
320-33F	LAN adapter
378-37F	Parallel printer port 1 (LPT 1)
380-38F	SDLC, bisynchronous
3A0-3AF	Bisynchronous
3B0-3BF	Monochrome display and printer port 3 (LPT 3)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)

1.4.2 Real-Time Clock and Non-Volatile RAM

The MBM-530NS contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

1.4.3 Timer

The MBM-530NS provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

1.5 Serial Port

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, 1.5 (in a five-bit format only) or two stop bits (in a 6,7, or 8-bit format). The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required handling the communications link.

The following table is a summary of each ACE accessible register.

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

(1) Receiver Buffer Register (RBR)
Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)
Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: "0" if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)
Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(7) Line Status Register (LSR)
Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

(8) MODEM Status Register (MSR)
Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

1.6 Parallel Port

(1) Register Address

Port Address	Read/Write	Register
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

(2) Printer Interface Logic

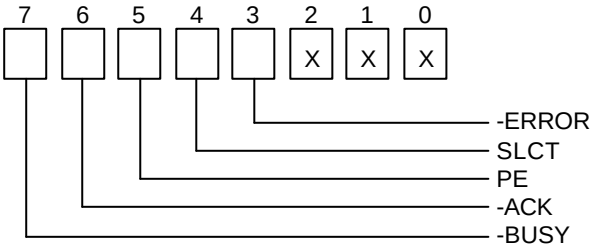
The parallel port of the NSPC87309 is for attaching various devices that accept eight bits of parallel data at standard TTL level.

(3) Data Swapper

The system microprocessor can read the contents of the printer' s Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:



NOTE: X presents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer' s ACK signal. A0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

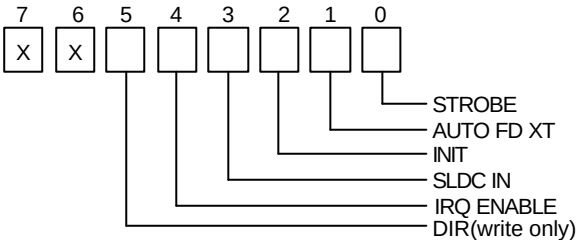
Bit 5: A1 means the printer has detected the end of the paper.

Bit 4: A1 means the printer is selected.

Bit 3: A0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:



NOTE: X presents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read. When logic 0, they work as a printer port. This bit is write only.

Bit 4: A1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A1 in this bit position selects the printer.

Bit 2: A0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A1 causes the printer to line-feed after a line is printed.

Bit 0: A0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

2. HARDWARE CONFIGURATION

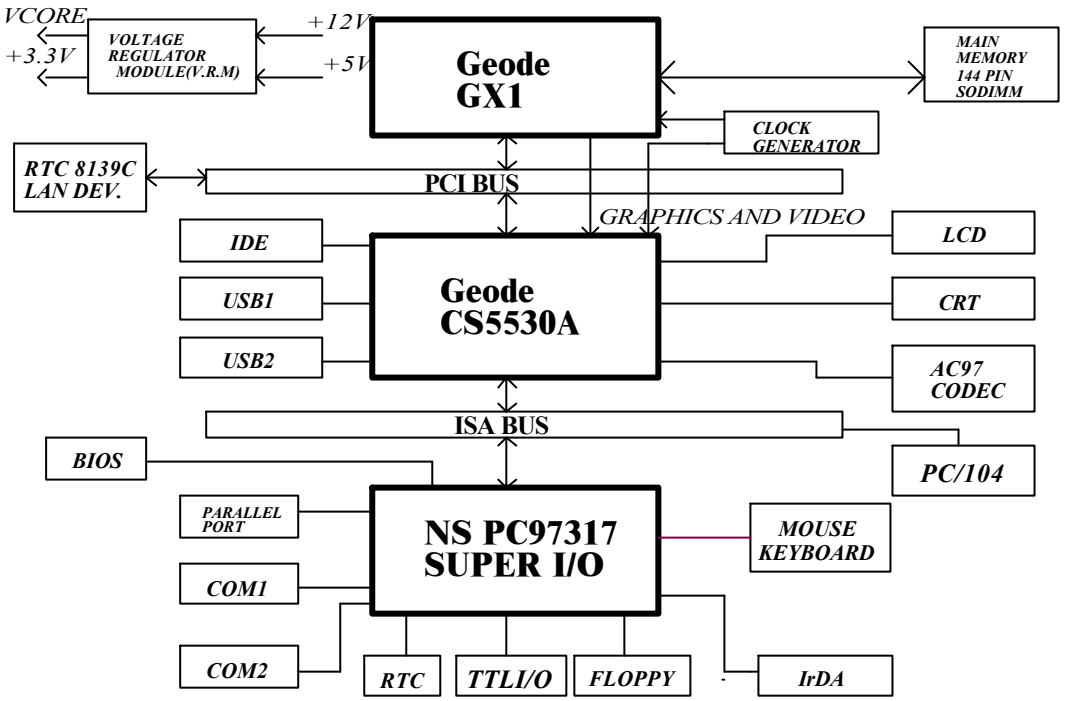
Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the MBM-530NS jumper pins, and the factory-default settings as below.

CAUTION: Do not touch any electronic components unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

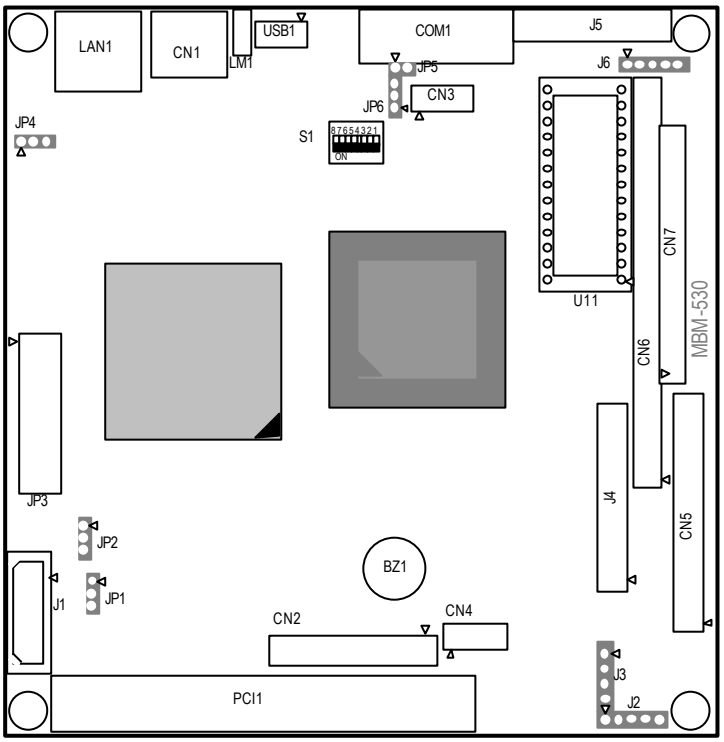
2.1 Jumper & Connector Quick Reference Table

2.2 Block Diagram



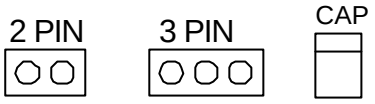
2.3 Component Locations

The MBM-530NS is an all-in-one Cyrix GXM-200 CPU board. This section provides the hardware' s jumper settings, the connectors' locations, and the pin assignments. The #1 pin assignments have all been designed on the right side of the board with a " block" indication on the diagram.



2.4 How to Set the Jumper

A jumper consists of two or three metal pins with a plastic base mounted on the card, and a small plastic cap (with a metal contact inside) to connect the pins, so you can set up your hardware configuration by "open" or close the pins. The jumper can be combined into sets, which called jumper blocks. When the jumpers are all in the block, you have to put them together to set up the hardware configuration. The figure below shows how it looks.



Jumpers and Cap

If a jumper has three pins, for example, labeled PIN1, PIN2, and PIN3, you can either connect PIN1 & PIN2 to create one setting and shorting or connect PIN2 & PIN3 to create another setting. The jumper setting rules are applied throughout this manual.

2.5 System Clock Select and CPU Setting

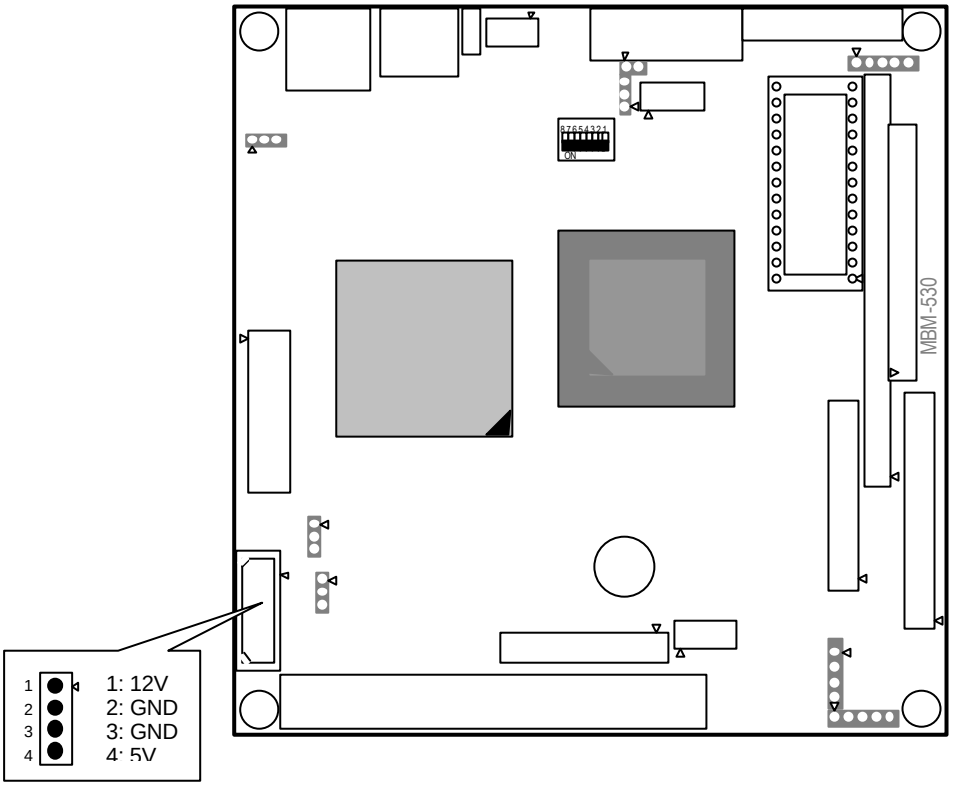
Table 1: CPU Core versus Core Frequency Characteristics

CPU GX1 Series	Core Voltage	System Clock	Freq. Multiplier	Core Freq.
300B-85-2.0	2.0V	33MHz	X9	300MHz

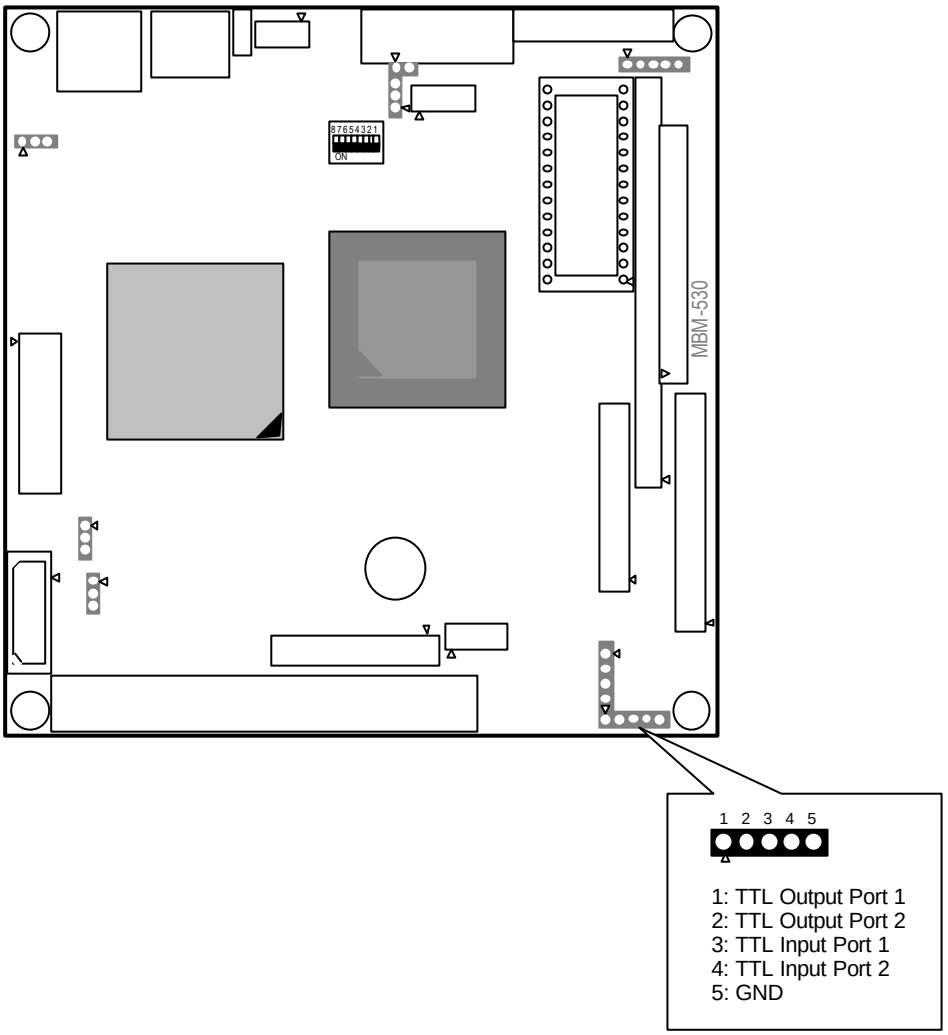
2.6 Jumper Setting

J1: Power Connector

The J1 is a 4-pin power connector; it connects the power +5V and +12V to apply MBM-530NS power.



J2: TTL I/O



TTL Input Demo Program

```
#include <stdio.h>

#include <stdlib.h>

#include <dos.h>


#define GPIO20    0x01                    //GPIO20
```

```
unsigned    Index_Reg = 0x002E, Data_Reg = 0x002F;
unsigned  char Dev_Index = 0x07, GPIO_Num = 0x07, PM_Num = 0x08;
unsigned   char  tmpData;


void main(void) {
   unsigned char
mBAR,lBAR,PM_Index_Reg,PM_Data_Reg,GPIO_En,port_Select,CFGDAT;
   unsigned  PMBAR,GPIOBAR;


   outportb(Index_Reg,  Dev_Index);       //Choose Logical Dev. PM
   outportb(Data_Reg,  PM_Num);                //
   outportb(Index_Reg,  0x30);             //Enable PM register access
   outportb(Data_Reg,  0x01);              //
   outportb(Index_Reg,  0x60);             //PM Base address MSB
   mBAR = inportb(Data_Reg);               //
   outportb(Index_Reg,  0x61);             //PM Base address LSB
   lBAR = inportb(Data_Reg);               //
  PMBAR = ((unsigned)mBAR <<8) + ((unsigned)lBAR);
   PM_Index_Reg = inportb(PMBAR + 0x00);       //GPIO ports function
enable
  PM_Data_Reg = inportb(PMBAR + 0x01);         //
   outportb(PM_Index_Reg,  0x01);              //
   GPIO_En = inportb(PM_Data_Reg);             //
   outportb(PM_Index_Reg,  0x01);              //
   outportb(PM_Data_Reg,  (GPIO_En | 0x80));     //
```

```
   outportb(Index_Reg, Dev_Index);       //Choose Logical Dev. GPIO
   outportb(Data_Reg, GPIO_Num);              //
   outportb(Index_Reg, 0x30);            //Enable GPIO register access
   outportb(Data_Reg, 0x01);             //
   outportb(Index_Reg, 0x60);            //GPIO Base address MSB
   mBAR = inportb(Data_Reg);             //
   outportb(Index_Reg, 0x61);            //GPIO Base address LSB
   lBAR = inportb(Data_Reg);             //
   GPIOBAR = ((unsigned)mBAR <<8) + ((unsigned)lBAR);

/*********************************************************/
/* Read from GPIO20 and check its status                 */
/*********************************************************/
   outportb(Index_Reg, 0x22);            //GPIO Bank select
   port_Select = inportb(Data_Reg);      //
   outportb(Index_Reg, 0x22);            //GPIO port2 select
    outportb(Data_Reg,(port_Select & 0x7F)); //
   outportb((GPIOBAR + 0x05), 0x80);          //set port2 input direction
   tmpData = inportb(GPIOBAR + 0x04) & GPIO20;
   if (tmpData == GPIO20) printf("GPIO20 is at HIGH state\n");
   else printf("GPIO20 is at LOW state.\n");

}
```

TTL Output Demo Program

```
#include <stdio.h>

#include <stdlib.h>

#include <dos.h>


#define GPIO37 0x80                    //GPIO37


unsigned    Index_Reg = 0x002E, Data_Reg = 0x002F;

unsigned  char Dev_Index = 0x07, GPIO_Num = 0x07, PM_Num = 0x08;

unsigned   char  tmpData;


void main(void) {

  unsigned  char
mBAR,lBAR,PM_Index_Reg,PM_Data_Reg,GPIO_En,port_Select,CFGDAT;

  unsigned  PMBAR,GPIOBAR;


  outportb(Index_Reg,  Dev_Index);       //Choose Logical Dev. PM

  outportb(Data_Reg,  PM_Num);                 //

  outportb(Index_Reg,  0x30);              //Enable PM register access

  outportb(Data_Reg,  0x01);               //
```

```
  outportb(Index_Reg, 0x60);              //PM Base address MSB
  mBAR = inportb(Data_Reg);               //
  outportb(Index_Reg, 0x61);              //PM Base address LSB
  lBAR = inportb(Data_Reg);               //
  PMBAR = ((unsigned)mBAR <<8) + ((unsigned)lBAR);
  PM_Index_Reg = inportb(PMBAR + 0x00);       //GPIO ports function
enable
  PM_Data_Reg = inportb(PMBAR + 0x01);        //
  outportb(PM_Index_Reg, 0x01);               //
  GPIO_En = inportb(PM_Data_Reg);             //
  outportb(PM_Index_Reg, 0x01);               //
   outportb(PM_Data_Reg, (GPIO_En | 0x80));    //


  outportb(Index_Reg, Dev_Index);       //Choose Logical Dev. GPIO
  outportb(Data_Reg, GPIO_Num);               //
  outportb(Index_Reg, 0x30);            //Enable GPIO register access
  outportb(Data_Reg, 0x01);             //
  outportb(Index_Reg, 0x60);            //GPIO Base address MSB
  mBAR = inportb(Data_Reg);             //
  outportb(Index_Reg, 0x61);            //GPIO Base address LSB
```

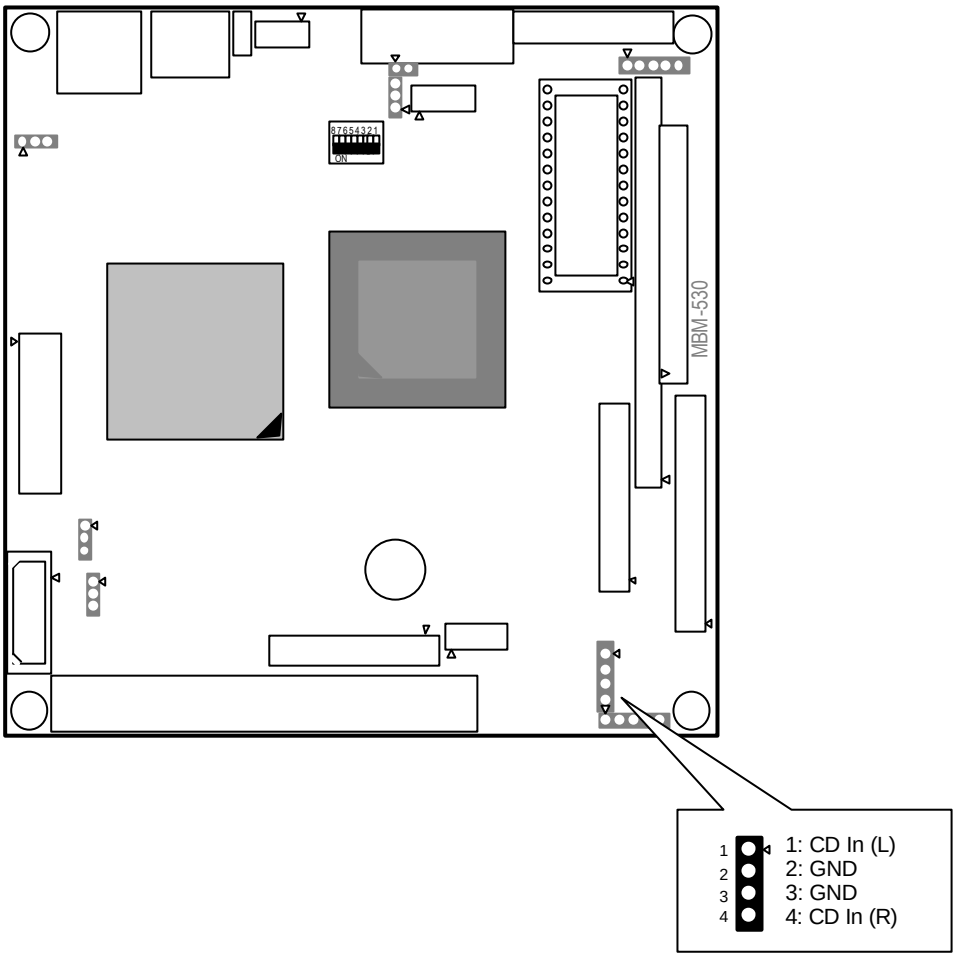
```
  lBAR = inportb(Data_Reg);                //

  GPIOBAR = ((unsigned)mBAR <<8) + ((unsigned)lBAR);


/*******************************************************/
/* Outport 1 to GPIO37                                 */
/*******************************************************/
   outportb(Index_Reg, 0x22);              //GPIO Bank select
   port_Select = inportb(Data_Reg);        //
   outportb(Index_Reg, 0x22);              //GPIO port3 select
   outportb(Data_Reg, (port_Select | 0x80));   //
  outportb((GPIOBAR + 0x05), 0x80);          //set port3 output direction
  tmpData = inportb(GPIOBAR + 0x04);
  outportb((GPIOBAR + 0x04),(tmpData | GPIO37));//GPIO37 = 1
  tmpData = inportb(GPIOBAR + 0x04) & GPIO37;
  if (tmpData != GPIO37) printf("GPIO37 is at LOW status.\n");
  else printf("GPIO37 is at HIGH status.\n");
}
```

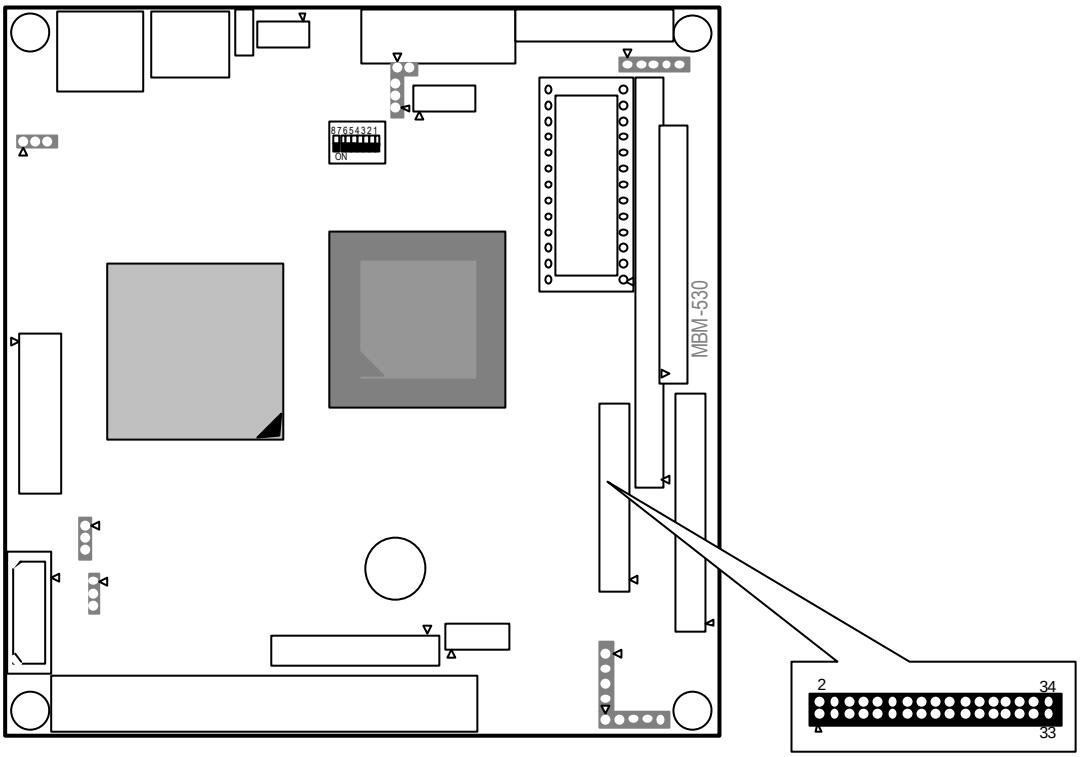
J3: CD Audio in Connector

The J3 is used to connect to a multi sound panel connector .It consist of a line in, a line out, and a microphone



J4: Floppy Connector

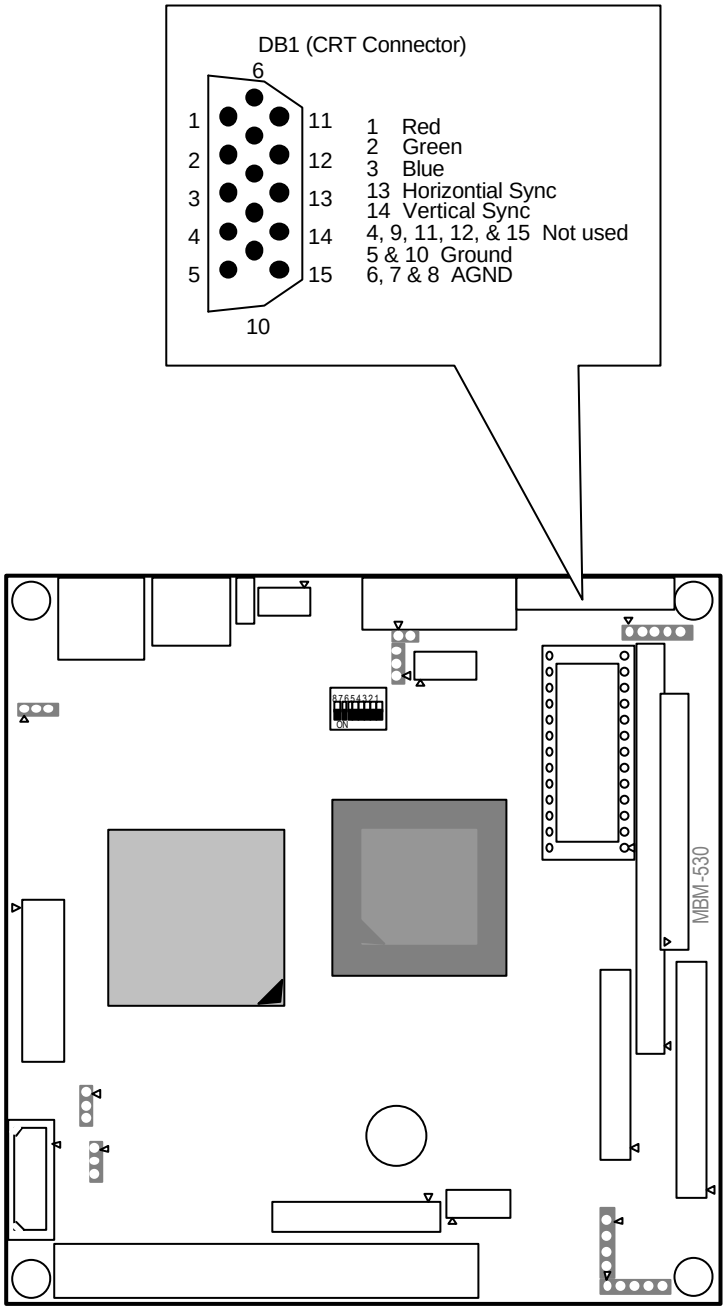
It provides a 34-pin header type connector for supporting up to two floppy disk drives in a daisy chain style. The last connector on the cable is the master.



Pin	Signal	Pin	Signal
1-33 (odd)	GROUND	18	-DIRECTION
2	-REDUCED WRITE CURRENT	20	-STEP OUTPUT PULSE
4	NOT USED	22	-WRITE DATA
6	NOT USED	24	-WRITE ENABLE
8	-INDEX	26	-TRACK 0
10	-MOTOR ENABLE A	28	-WROTE PROTECT
12	-DRIVE SELECT B	30	-READ DATA
14	-DRIVE SELECT A	32	-SIDE 1 SELECT
16	-MOTOR ENABLE B	34	-DISK CHANGE

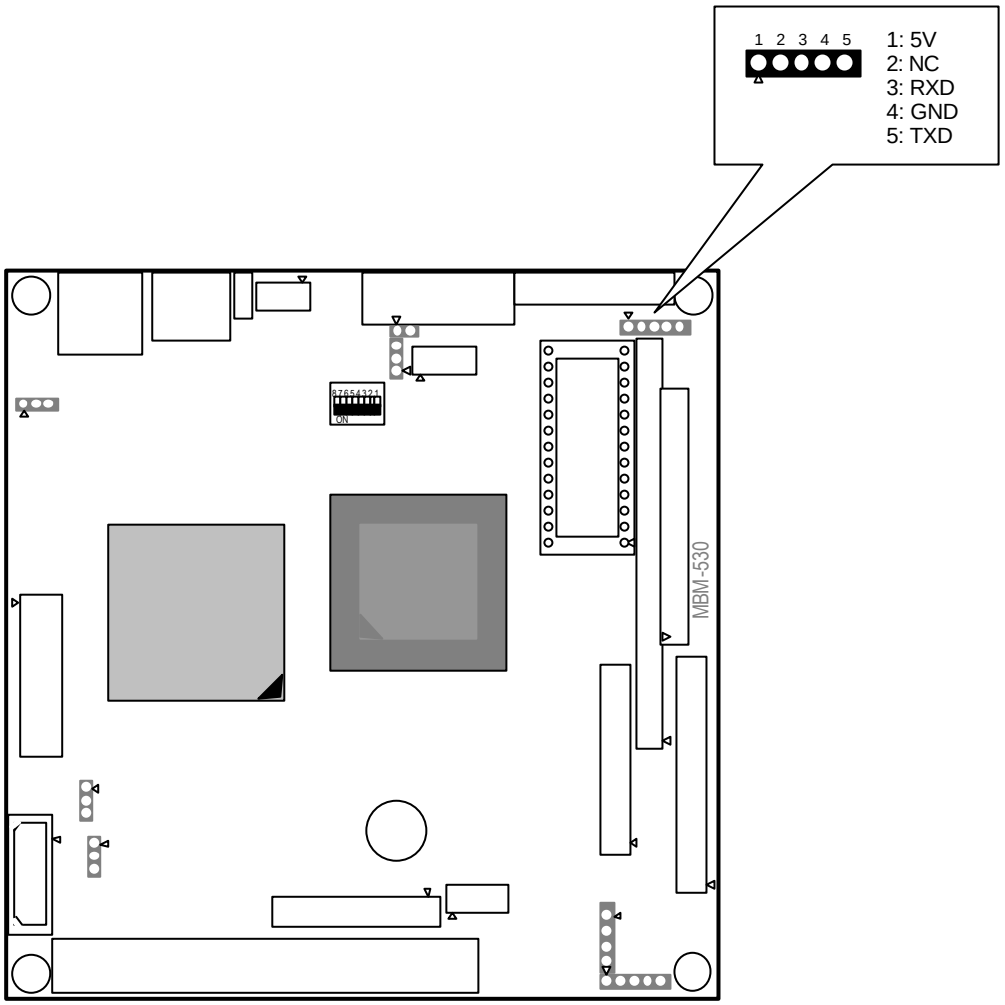
J5: VGA Connector D-SUB

J5 is used to connect with a VGA monitor when you are using the on-board VGA controller as the display adapter. Pin assignments for the J5 connector are as follows:

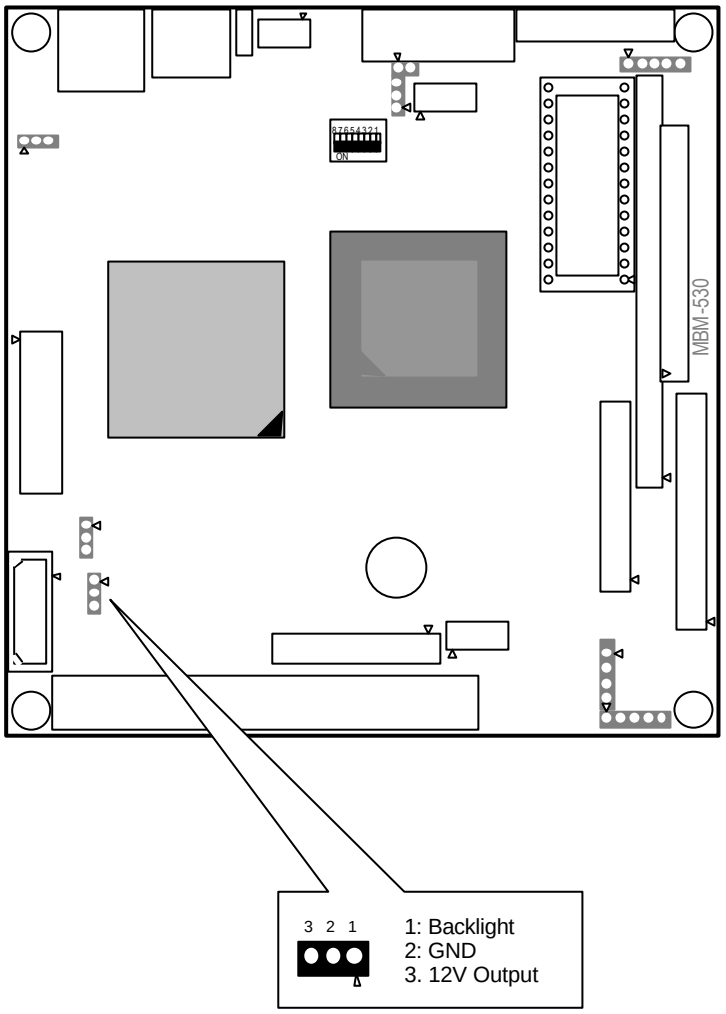


J6: IrDA Connector

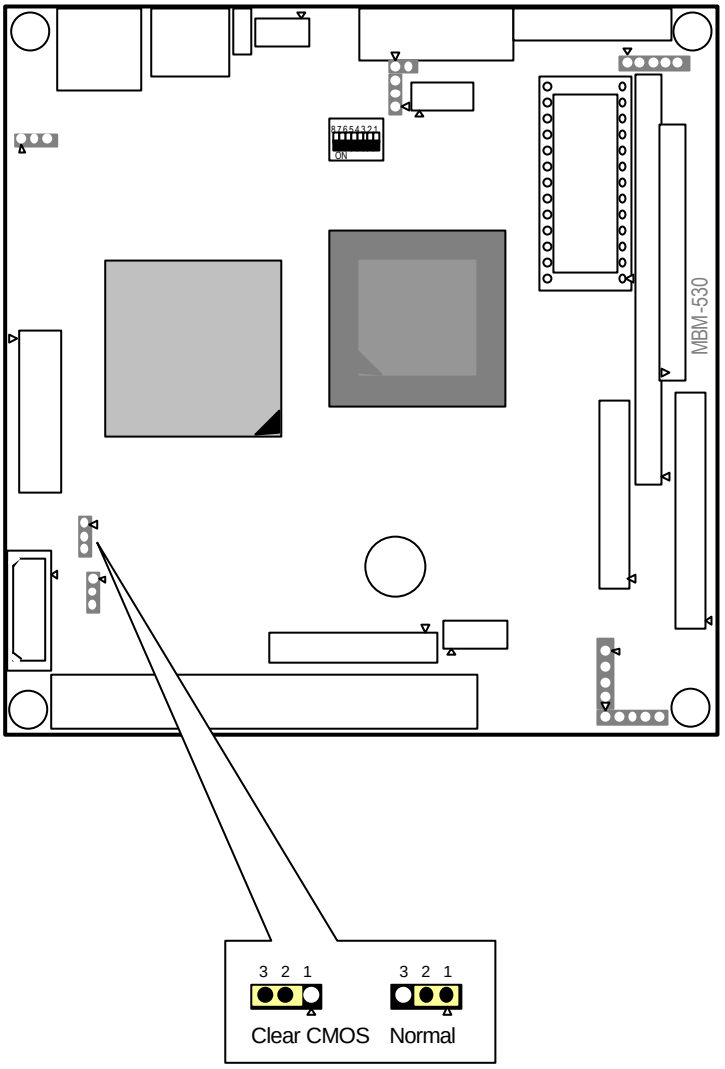
When using the internal IrDA header it will automatically become COM 2. This means that COM 2 will not be able to be used as a serial connection. This selection should be selected in the BIOS (The best setting is to use “ Standard”).



JP1: LCD Backlight Control

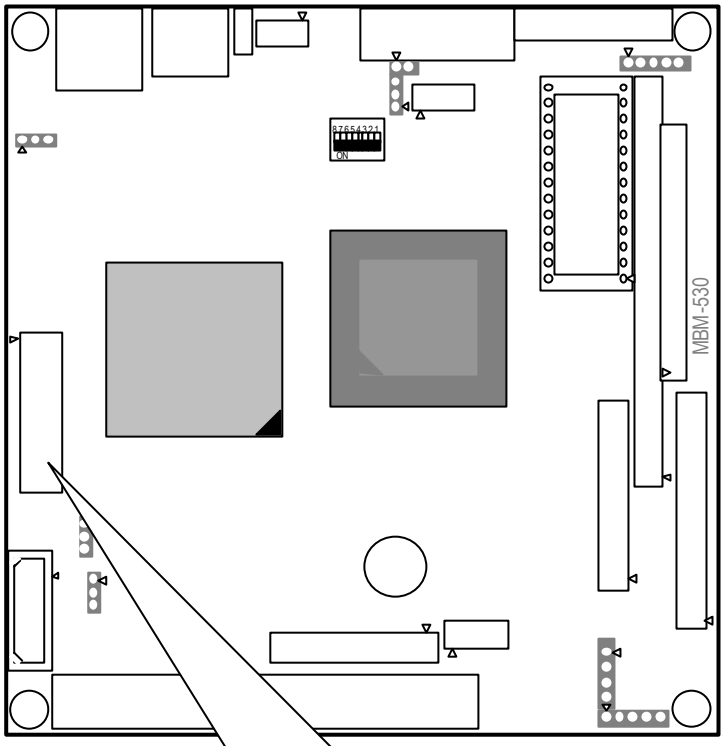


JP2: CMOS Clear



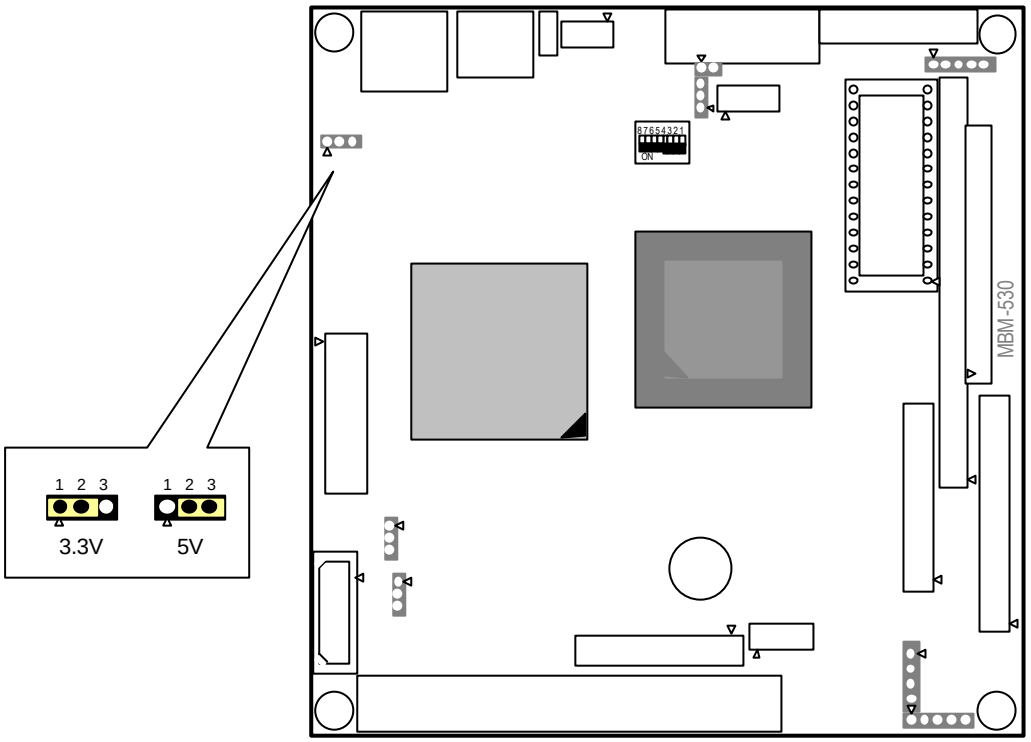
JP3: LCD Connector

You may attach a display panel connector to this 40-pin connector with pin the assignments as shown below:



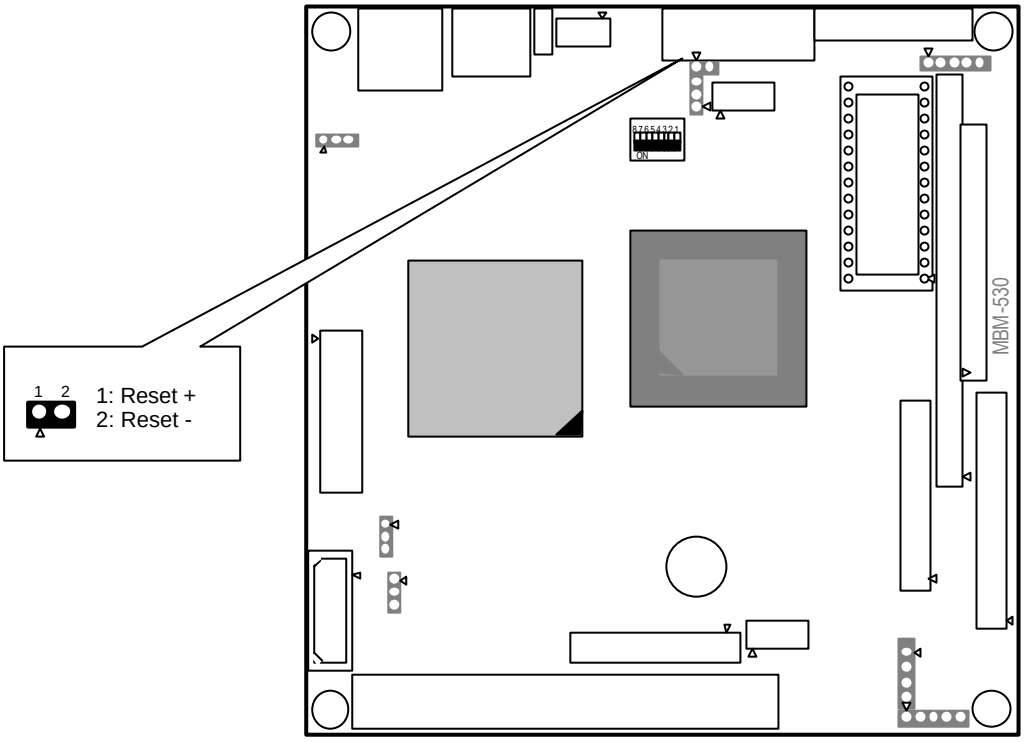
1: LCD Power VDD	21: D10
2: GND	22: D11
3: FPCLK	23:LCD Power VDD
4: GND	24: D12
5: GND	25: D13
6: PPHSYNC	26: D14
7: FPVSYNC	27: D15
8: M Signal	28: GND
9: D16	29: D0
10: D17	30: D1
11: NC	31: D2
12: NC	32: D3
13: GND	33: GND
14: NC	34: D4
15: NC	35: D5
16: NC	36: D6
17: NC	37: D7
18: GND	38: LCD Power VDD
19: D8	39: Output Enable
20: D9	40: LCD Power VDD

JP4: LCD Power VDD Select

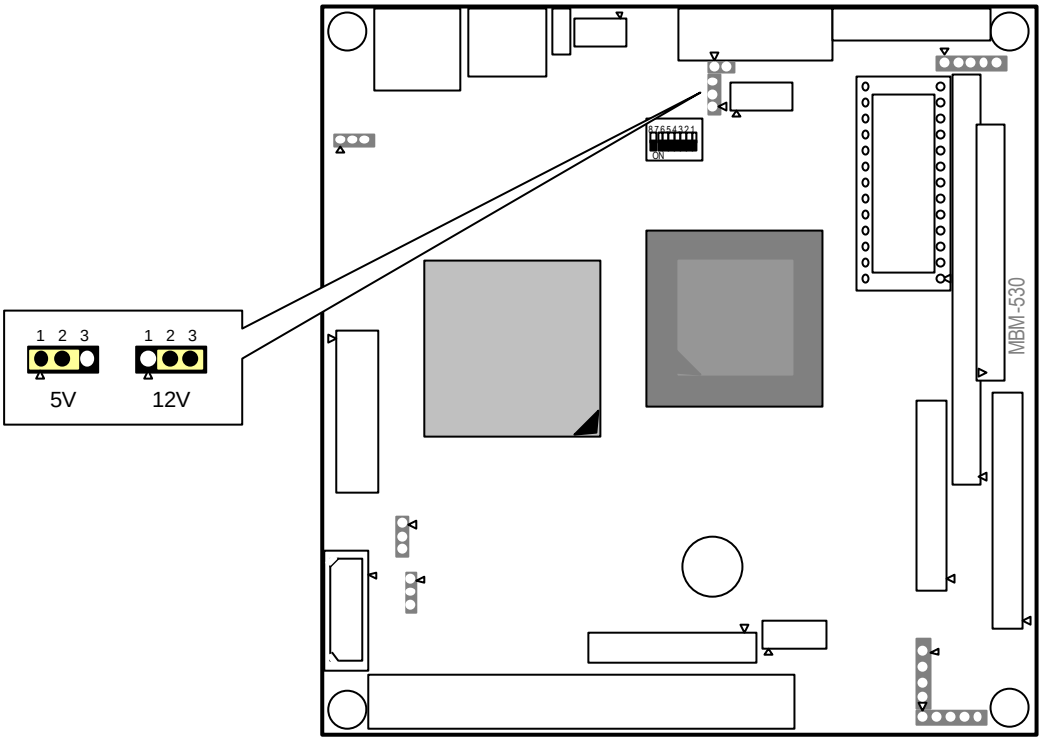


JP5: External Reset Switch

The switch is act as the MBM-530NS system reset control. The extra reset control can be done by JP5, which connect to an external reset switch. Shorting these two pins will reset the system.



JP6: COM2 Power Select

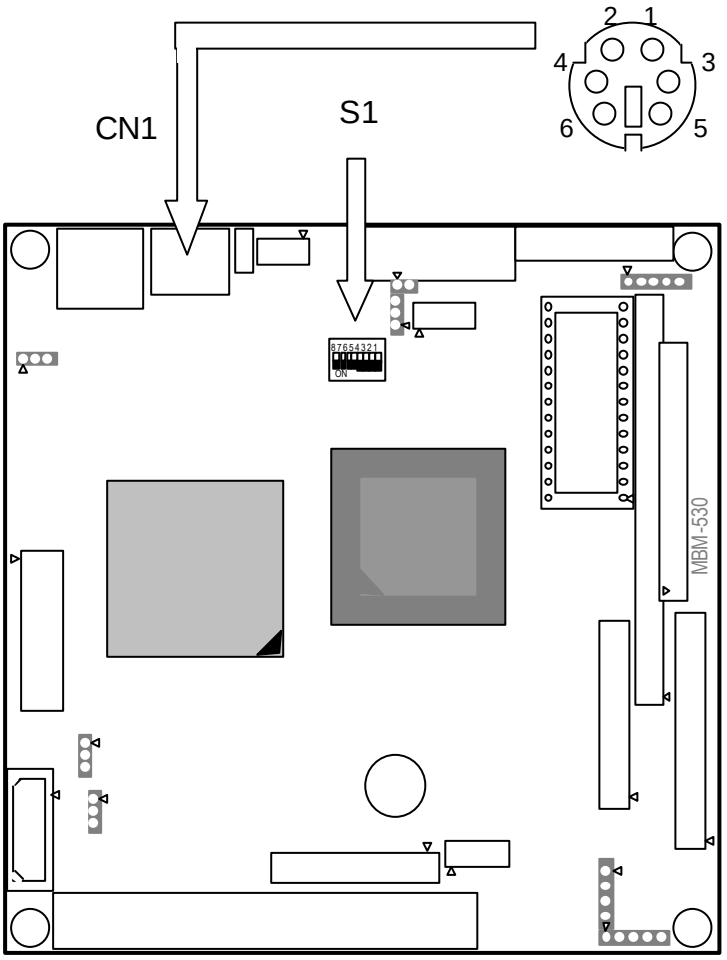


S1: COM2 RS-232, RS-422, RS-485 Selection

The RS-232C interface on the MBM-530NS is used DSUB-9 COM port connector (COM1). COM2 uses on-board 10-pin pinhead connectors (CN3). To configure them, use the BIOS Setup program (covered later section). The switch S1 for choosing between RS-232, RS-422 and RS-485 can adjust COM 2.

Function	1	2	3	4	5	6	7	8
RS-232	Off	Off	Off	Off	Off	Off	Off	Off
RS-422	On	On	On	On	On	On	On	Off
RS-485	On	Off	On	On	On	On	On	On

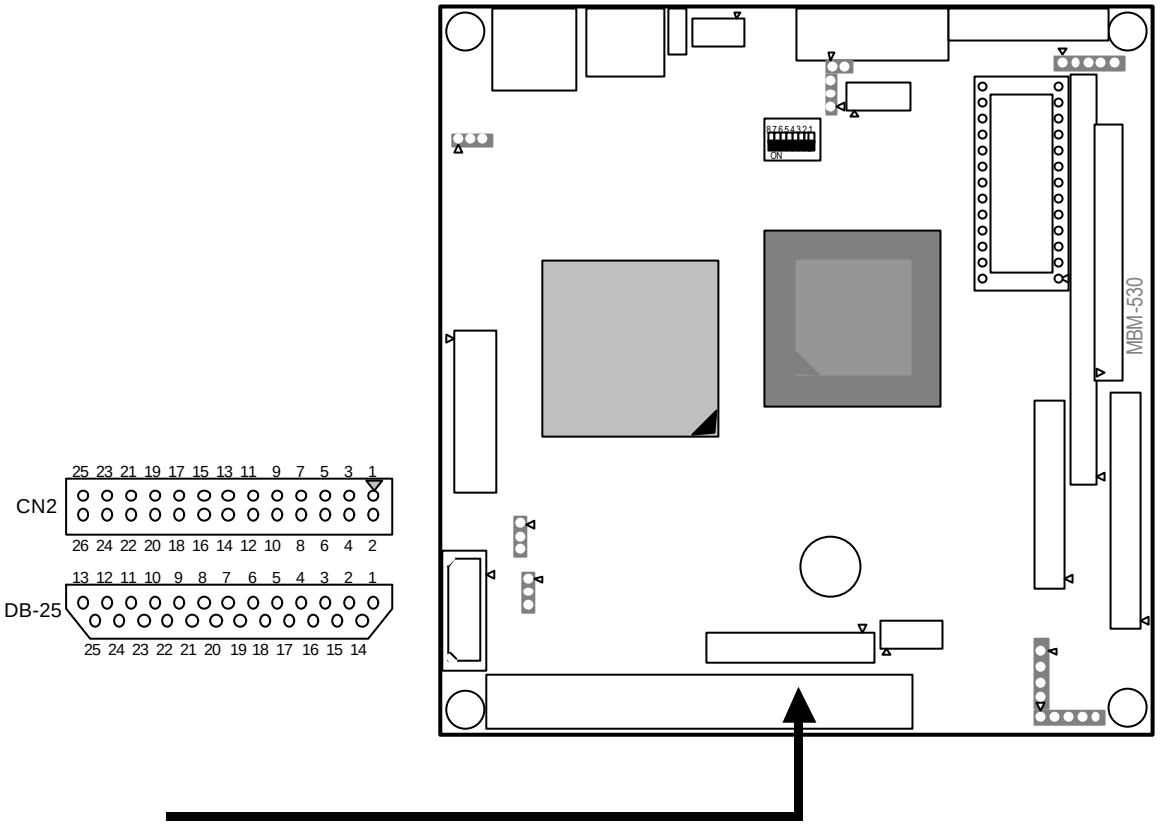
CN1: PS2 Keyboard / Mouse



Pin	PS/2 Keyboard Pin Assignment
1	KDAT
2	MDAT
3	KMGD
4	KMVCC
5	KCLK
6	MCLK

CN2: Printer Port

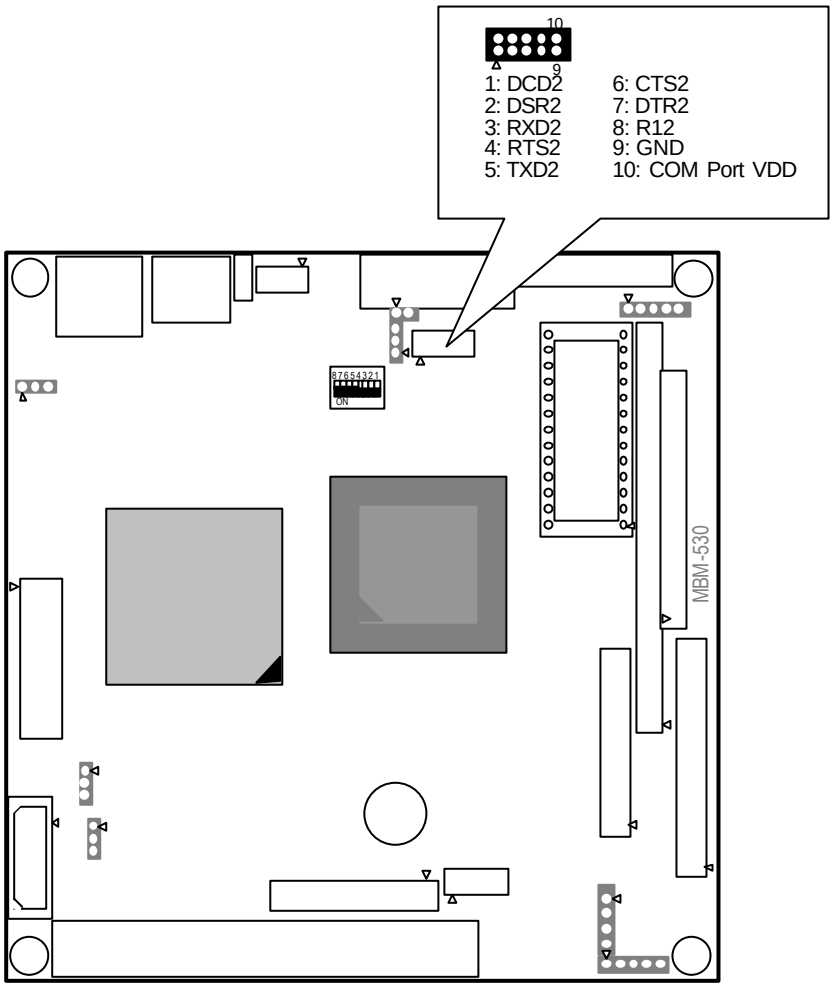
To use the parallel port, an adapter cable has been connected to the CN2 (26-pin header type) connector. This adapter cable is mounted on a bracket and is included in your MBM-530NS package. The connector for the parallel port is a 25-pin D-type female connector.



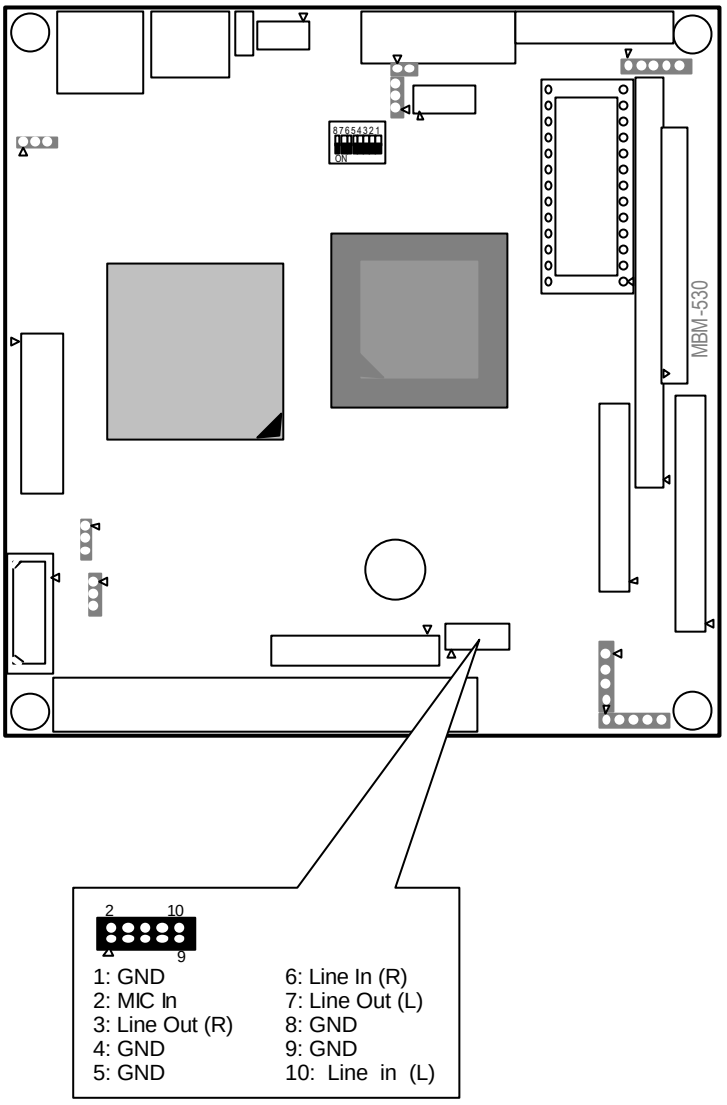
CN2	DB-25	Signal	CN2	DB-25	Signal
1	1	-Strobe	2	14	-Auto Form Feed
3	2	Data 0	4	15	-Error
5	3	Data 1	6	16	-Initialize
7	4	Data 2	8	17	-Printer Select In
9	5	Data 3	10	18	Ground
11	6	Data 4	12	19	Ground
13	7	Data 5	14	20	Ground
15	8	Data 6	16	21	Ground
17	9	Data 7	18	22	Ground
19	10	-Acknowledge	20	23	Ground
21	11	Busy	22	24	Ground
23	12	Paper	24	25	Ground
25	13	Printer Select	26	--	Not Used

CN3: COM2 Connector

The RS-232C interface on the MBM-530NS is used DSUB-9 COM port connector (COM1). COM2 uses on-board 10-pin pinhead connectors (CN3). To configure them, use the BIOS Setup program (covered later section). The switch S1 for choosing between RS-485, RS-422 and RS-232C can adjust COM 2.

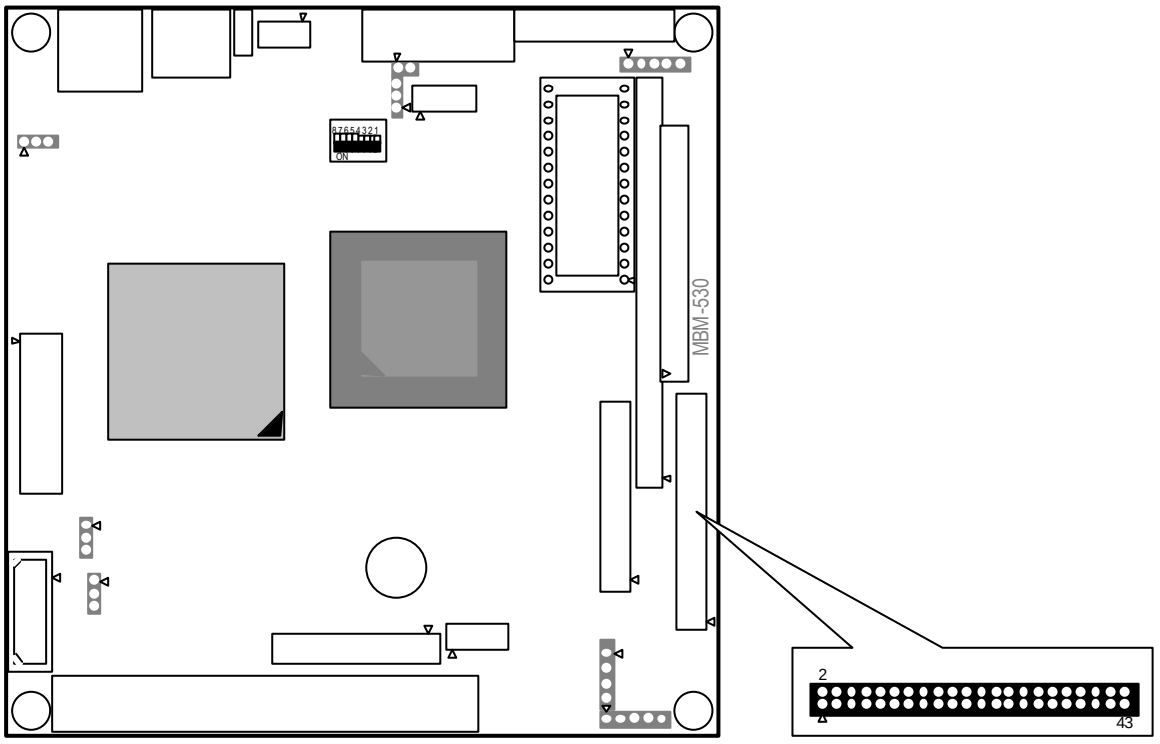


CN4: Multi Sound Panel Connector



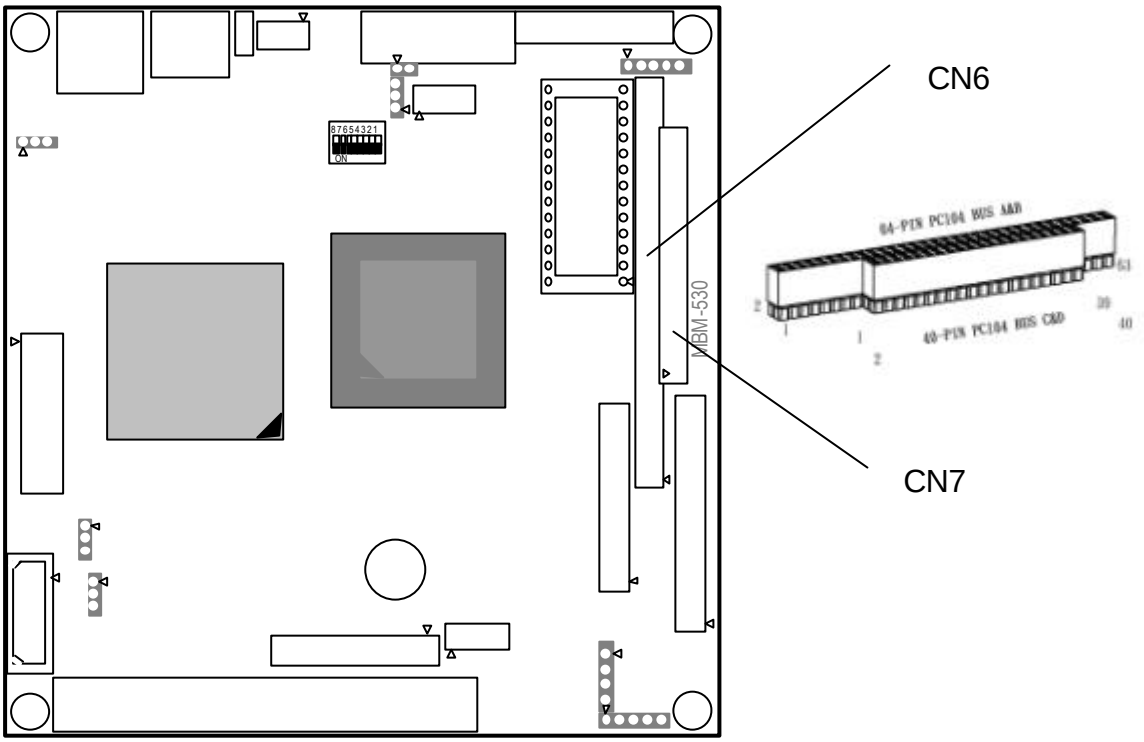
CN5: Hard Disk Connector

A 44-pin header type connector (CN5) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 44-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use the BIOS Setup program, which is explained in further section. The following table illustrates the pin assignments of the hard disk drive' s 44-pin connector. The last pin on the cable is the master.



PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	-RESET	2	GROUND	23	-LOW A	24	GROUND
3	DATA 7	4	DATA 8	25	-LOR A	26	GROUND
5	DATA 6	6	DATA 9	27	-CHRDY A	28	GROUND
7	DATA 5	8	DATA 10	29	DACKA	30	GROUND
9	DATA 4	10	DATA 11	31	-IRQ 14	32	NOT USED
11	DATA 3	12	DATA 12	33	SA 1	34	NOT USED
13	DATA 2	14	DATA 13	35	SA 0	36	SA2
15	DATA 1	16	DATA 14	37	CS 0	38	SA1
17	DATA 0	18	DATA 15	39	HD LED A	40	NOT USED
19	GROUND	20	NOT USED	41	VCC	42	VCC
21	IDEDRQA	22	GROUND	43	GROUND	44	GROUND

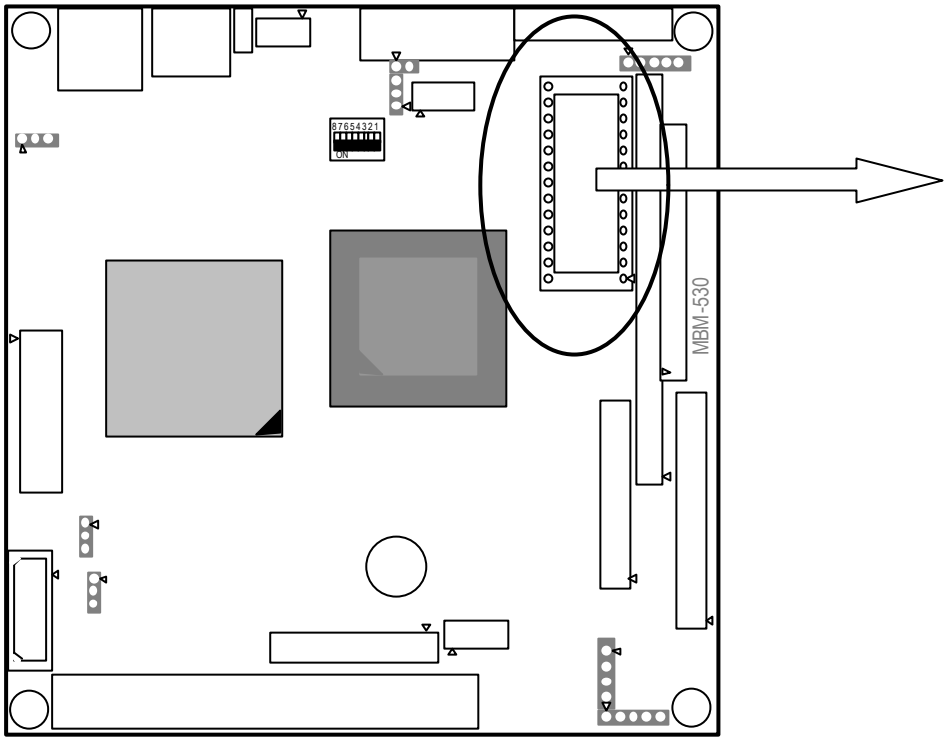
CN6 & CN7: PC-104 Connector



Name	Description	Name	Description
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.	**-SMEMW** [Output]	The System Memory Write is low while any of the low 1 mega bytes of memory is being written
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset	**-MEMW** [Input/Output]	The Memory Write signal is low while any memory location is being written
SA0 - SA19 [Input/Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"	**DRQ 0-3, 5-7** [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
LA17- LA23 [Input/Output]	The Unlatched Address line run from bit 17 to 23	**-DACK 0-3, 5-7** [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7

Name	Description	Name	Description
SD0-SD15 [Input/Output]	System Data bit 0 to 15	**AEN** [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
BALE [Output]	The Buffered Address Latch Enable is used to latch SA0 - SA19 onto the falling edge. This signal is forced high during DMA cycles	**-REFRESH** [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board	**TC** [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
IOCHRDY [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address	**SBHE** [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)	**-MASTER** [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus	**-MEMCS16** [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus	**-IOCS16** [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
-SMEMR [Output]	The System Memory Read is low while any of the low 1 mega bytes of memory are being used	**OSC** [Output]	The Oscillator is a 14.31818 MHz signal used for the color graphic card
-MEMR [Input/Output]	The Memory Read signal is low while any memory location is being read	**-ZWS** [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

U11: DiskOnChip Socket



DOC Memory Address Select

This section provides the information about how to use the DOC (DiskOnChip).

1. The address of DiskOnChip is DC000H.
2. Insert programmed DiskOnChip into socket U11 setting as DOC.

3. SOFTWARE UTILITY

3.1 Driver File List

There are three directories in the MBM-530NS Driver CD. Following is the details of every directory.

RSET8139 [DIR]

8139c.cfg	pg8139.exe	rset8139.exe

VGAAUDIO [DIR]

cryix.exe	license.pdf

RTL8139 [DIR]

Brom[DIR]	Client32[DIR]	Dmi[DIR]	Freebsd[DIR]
Linux[DIR]	Macos[DIR]	Mslanman.dos[DIR]	Mslanman.Os2[DIR]
Ndis2Dos[DIR]	Ndis2Os2[DIR]	Nt351[DIR]	Nwclient[DIR]
Nwserver[DIR]	Rtos[DIR]	Rtspkt[DIR]	Sco[DIR]
Txt[DIR]	Uw7[DIR]	W95Osr2[DIR]	Wfm311[DIR]
Win2000[DIR]	Win95a[DIR]	Win98[DIR]	Windiag[DIR]
Winnt4[DIR]	Diskdir.txt	Filepath.lst	Help8139.exe
Mainmenu.txt	Netrts.inf	Netrts_a.___	Netrts5.___
Oemsetup.inf	Rset8139.exe	Version.txt	

3.2 Install VGA and Audio Driver

The MBM-530NS provides video and audio function drivers for the WIN95 and WIN98, the driver can auto-setup in the WIN95 or WIN98 mode.

1. Change directory to the **[VgaAudio]**.
2. Execute the file **Cryix.exe**, the system will auto setup the video and audio functions.

3.3 Install Network Utility

1. Change directory to the [**Rtl8139**].
2. Choose the proper driver for your operating system.
3. Change directory to the [**Rset8139**]. You can configure and test your network function by following files.

8139c.cfg	- Configure LAN function
pg8139.exe	- LAN configuration EEPROM Programmer
rset8139.exe	- Diagnostic and modification program

4. BIOS SETUP

The following topics are covered in this section:

- **BIOS Configuration**
- **Standard CMOS Features**
- **BIOS Features Setup**
- **Chipset Features Setup**
- **Power Management Setup**
- **PnP/PCI Configurations**
- **Load BIOS Defaults**
- **Load Setup Defaults**
- **Integrated Peripherals Features Setup**
- **Supervisor/User Password Setting**
- **IDE HDD Auto Detection**
- **Save & Exit Setup**
- **Exit Without Saving**
- **Flash BIOS Writer Utility**

4.1 BIOS Configuration

This chapter contains the explanation of the system BIOS and instructions on configuring the system by setting the BIOS parameters. Because the BIOS code is the most often changed part of the SBC design, the BIOS information contained in this chapter (especially the Chipset Setup parameters) may be a little different compared to the actual BIOS that came with your SBC. The screen contents in this chapter are provided as examples only and may not reflect the screen contents displayed on your system.

4.1.1 Award BIOS

The MBM-530NS SBC is equipped with an AWARD BIOS (Basic Input and Output System). The BIOS setup utility is a segment of codes/routines residing in the BIOS Flash ROM. (The SBC supports a programmable Flash ROM chip, 3 Volt. This memory chip can be updated when BIOS upgrades are released.) This built-in routine allows you to configure the system parameters and then save the configuration into the 256 bytes CMOS area in the BIOS ROM. The BIOS ROM is battery-backed so that it retains the Setup information even when the power is turned off.

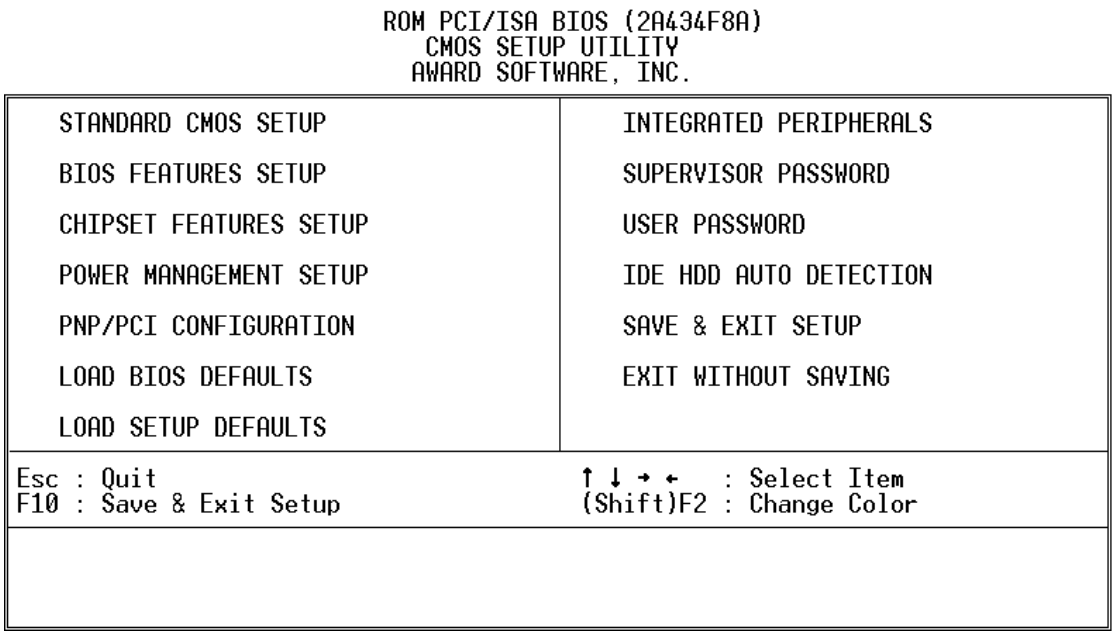
BIOS plays a role of bridging the system hardware and the operating system. When you first power on the SBC, the BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks, launch, and let operating system take over the control.

Every SBC provides a Setup utility program for specifying the system configuration and settings. If your SBC came in a computer system, the proper configuration entries may have already been made. If so, invoke the Setup utility, as described later, and take note of the configuration settings for future reference, In particular, the hard disk specifications.

4.1.2 Entering the Award BIOS Setup Menu

When you turn on the computer, the system provides you with the opportunity to run this program. This appears during the Power-On Self Test (POST). Press <delete> to call up the Setup utility. If you are a little bit late pressing the mentioned key(s), POST will continue with its test routines, thus preventing you from calling up Setup. If you still need to call Setup, reset the system by pressing <Ctrl>+<Alt>+<Delete>, or by pressing the Reset button on the system case. You can also restart by turning the system off and then back on again. Do it only if the first two methods fail. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to **PRESS F1 TO CONTINUE, DEL TO ENTER SETUP**.

After you hold down <DEL> and then enter the BIOS CMOS Setup Utility, the CMOS SETUP UTILITY main program screen will appear with the following options. This Main Menu contains several setup options and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.



BIOS Setup Main Menu

4.1.3 BIOS CONFIGURATION

The section at the bottom of the above screen tells how to control the screen. Take note of these keys and their respective uses. Another section just below control keys section displays a brief description of the currently highlighted item in the list.

- **Standard CMOS setup**
  This setup page includes all the items in standard compatible BIOS.
- **BIOS features setup**
  This setup page includes all the items of Award special enhanced features.
- **Chipset features setup**
  This setup page includes all the items of chipset special features.
- **Power management setup**
  This setup page includes all the items of Green function features.
- **PNP/PCI configuration**
  This setup page includes all the configurations of PCI & PnP ISA resources.
- **Load BIOS defaults**
  BIOS Defaults indicates the most appropriate value of the system parameters that system would be in safe configuration.
- **Load Setup defaults**
  Performance Defaults indicates the value of the system parameters that the system would be in the best performance configuration.
- **Integrated peripherals**
  This setup page includes all onboard peripherals.
- **Supervisor password**
  Change, set, or disable password. It allows you to limit access to the system and Setup, or just to Setup
- **User password**
  Change, set, or disable password. It allows you to limit access to the system
- **IDE HDD auto detection**
  Automatically configure hard disk parameters.
- **Save & exit setup**
  Save CMOS value settings to CMOS and exit setup.
- **Exit without saving**
  Abandon all CMOS value changes and exit setup.

Control Keys

In general, you use the arrow keys to highlight items, press <Enter> to select, use the <PageUp> and <PageDown> keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more details about how to use the keyboard.

< ↑ >	Move to previous item, to select items
< ↓ >	Move to next item, to select items
<← >	Move to the item in the left hand, to select items
<→>	Move to the item in the right hand, to select items
<ESC>	Main Menu: To exit BIOS utility, Quit and not save change into CMOS Status Page Setup Menu and Option Page Setup Menu: to exit current page and return to Main Menu
<PageUp>	Increase the numeric value or make changes modify parameters.
<PageDown>	Decrease the numeric value or make change; modify parameters.
<+>	Increase the numeric value or make changes; modify parameters.
<->	Decrease the numeric value or make change; modify parameters.
<F1>	To find general help, only for Status Page Setup Menu and Option Page Setup Menu.
<Shift>+<F2>	Change color from total 16 colors. <F2> to select color forward, <Shift>+<F2> to select color backward.
<F3>	Calendar, only for Status Page Setup Menu
<F4>	Reserved
<F5>	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu.
<F6>	Load the default CMOS value from BIOS default table, only for Option Page Setup menu.
<F7>	Load the default
<F8>	Reserved
<F9>	Reserved
<F10>	Save all the CMOS changes, only for Main menu

Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. The SETUP Defaults are also noted in this Help Window to your reference. To exit the Help Window press <Esc> or the F1 key again.

In Case of Problems (Load BIOS Default)

If your computer can not boot after making and saving system changes with Setup, select the option "LOAD BIOS DEFAULTS" to load the minimum settings for troubleshooting or "LOAD SETUP DEFAULTS" to load optimised defaults for regular use. All applicable set-tings will be modified.

Note:

All BIOS defaults are marked in parenthesis next to each function title in this BIOS Setup manual.

Tips:

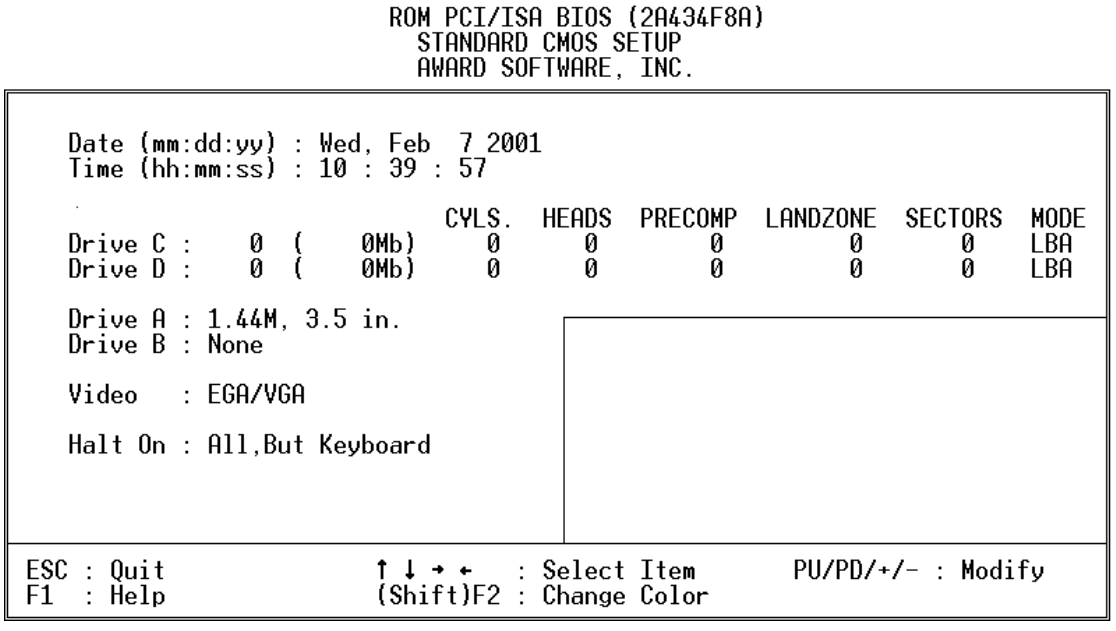
The best advice is to only alter settings, which you thoroughly understand. It is strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen to provide the absolute maximum performance and reliability. Even a slightest change to the chipset setup may jeopardize the booting of your system.

4.2 Standard CMOS Setup

The "Standard CMOS Setup" option allows you to record some basic system hardware con-figuration and set the system clock and error handling. If the configuration stored in the CMOS memory on SBC gets lost or damaged or if you change your system hardware configuration, you will need to re-specify the configuration values. The configuration values usually get lost or corrupted when the power of the onboard CMOS battery weakens. It will also get lost when you remove the CMOS battery from SBC.

Note:

The screen contents in this manual are provided as examples only and may not reflect the screen contents displayed on your system.



Standard CMOS Setup

The preceding screen provides you with a list of options. At the bottom of this screen are control keys. Take note of these keys and their respective uses.

User-configurable fields appear in a different color. If you need information in the selected field, press <F1>. The help menu will then appear to provide you with the information you need. The memory display at the lower right of the screen is read-only and automatically adjusts accordingly.

The items in Standard CMOS Setup Menu are divided into 10 categories. Each category includes several setup items. Use the arrow keys to highlight the item and then use the <PageUp> or <PageDown> keys to select the value for each item.

Details of Standard CMOS Setup

Date

To set date, highlight the "Date" field and then press <PageUp> / <PageDown> or <+>/<-> to set the current date. Follow the month, day and year format. Valid values for month, day and year are : Month: (1 to 12), Day: (1 to 31), Year: (up to 2079). Press <F3> to show the calendar.

day of the week	From Sun to Sat, determined by the BIOS and is only for display
day	From 1st to 31st(or the maximum allowed in the month)
month	From Jan. to Dec.
year	From 1900 to 2099

Time

To set the time, highlight the "Time" field and then press <PageUp> /<PageDown> or <+>/<->to set the current time. Follow the hour, minute and second format. Valid values for hour, minute and second are: Hour: (00 to 23), Minute: (00 to 59), Second: (00 to 59). The time is based on the 24-hour military-time clock. 1 p.m., for example, is 13:00:00.

Note:

You can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Hard Disks

This field records the specifications for all non-SCSI had disk drives installed in your system. The onboard PCI IDE connectors provide Primary and Secondary channels for connecting up to four IDE hard disks or other IDE devices. Each channel can support up to two hard disks; the first of which is the "master" and the second is the "slave".

Specifications for SCSI hard disks need not to be entered here since they operate using device drivers and are not supported by any of the BIOS. Please refer to the respective documentation of the devices.

For IDE hard disk drive setup, you can:

- Use the Auto setting for detection during bootup.
- Use the IDE HDD AUTO DETECTION in the main menu to automatically enter the driver' s specifications.
- Enter the specifications yourself manually by using the "User" option.

The entries for specifying the hard disk type include **CYLS** (number of cylinder). **HEAD** (number of read/write heads), **PRECOMP** (write precompensation), **LANDZ** (landing zone), **SECTOR** (number of sectors) and **MODE**. The **SIZE** field automatically adjusts according to the configuration you specify. The documentation that comes with your hard disk should provide you with the information regarding the drive specifications.

The **MODE** entry is for IDE hard disks only, and can be ignored for MFM and ESDI drives. This entry provides three options: Normal, Large, LBA, or Auto (see below). Set **MODE** to the normal for IDE hard disk drives smaller than 528MB; set it to LBA for drives over528MB that support Logical Block Addressing (LBA) to allow larger IDE hard disks; set it to Large for drives over 528MB that do not support LBA. Large type of drive can only be used with MS-DOS and is very uncommon. Most IDE drives over 528MB support the LBA mode.

Type	Drive Type
CYLS	Number of Cylinders
HEADS	Number of Heads
PRECOMP	Write Pre-Compensation
LANDOZONE	Landing Zone
SECTORS	Number of Sectors
MODE	Mode Type

Auto detection of hard disks on bootup

For each field: Primary Master, Primary Slave, Secondary Master, and Secondary Slave, you can select Auto under the TYPE AND mode FIELDS. This will allow you to change your hard disks (with the power off) and then power on without having to reconfigure your hard disk type.

If you use older hard disks that do not support this feature, then you must configure the hard disk in the standard method as described earlier by the "User" option.

Note:

After the IDE had disk drive information has been entered into BIOS, new IDE hard disk drives must be partitioned (such as with FDISK) and then formatted before data can be read from and write on. Primary IDE hard disk drives must have its partition set to active (also possible with FDISK).

Drive A (1.44Mb, 3.5in.)

The field records the types of floppy disk drives installed in your system. The available options for drive A are: 360K, 5.25in. 1.2M, 5.25in., 720K, 3.5in.; 1.44M, 3.5in.; 2.88M, 3.5in.; None.

None	No floppy drive installed
360K, 5.25 in	5-1/4 inch PC-type standard drive; 360 kilobyte capacity
1.2M, 5.25 in	5-1/4 inch AT-type high-density drive; 1.2 megabyte capacity
720K,3.5 in	3-1/2 inch double-sided drive; 720 kilobyte capacity
1.44M, 3.5 in	3-1/2 inch double-sided drive; 1.44 megabyte capacity
2.88M, 3.5 in	3-1/2 inch double-sided drive; 2.88 megabyte capacity

Drive B (None)

Video (EGA/VGA)

Set this field to the type of video display card installed in your system. The options are EGA / VGA, CGA40, CGA80. And MONO (for Hercules or MDA). If you are using a VGA or any higher resolution card, choose EGA / VGA.

EGA / VGA	Enhanced Graphics Adapter/Video Graphics Array. For EGA, VGA, SEGA, SVGA or PGA monitor adapters.
CGA 40	Color Graphics Adapter, power up in 40 column mode
CGA 80	Color Graphics Adapter, power up in 80 column mode
MONO	Monochrome adapter includes high-resolution monochrome adapters.

Halt on (All, But Keyboard)

This field determines which types of error will cause the system to halt. Choose from All Errors; No Errors; All, But Keyboard; All, But Diskette; and All, But Disk/Key.

No errors	The system boot will not be halted for any error that may be detected.
All errors	Whenever the BIOS detecting any non-fatal or fatal error, the system will be halted and you will be prompted.
All, But Keyboard	The system boot will not stop for a keyboard error; it will stop for all other errors.
All, But Diskette	The system boot will not stop for a disk error; it will stop for all other errors.
All, But Disk/ key	The system boot will not stop for a keyboard or disk error; it will stop for all other errors

Memory

This field is display only. The BIOS will automatically detect the total amount of memory during POST (Power On Self-Test).

Base Memory

The POST will determine the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 512K or 640K for system utilization.

Extended Memory

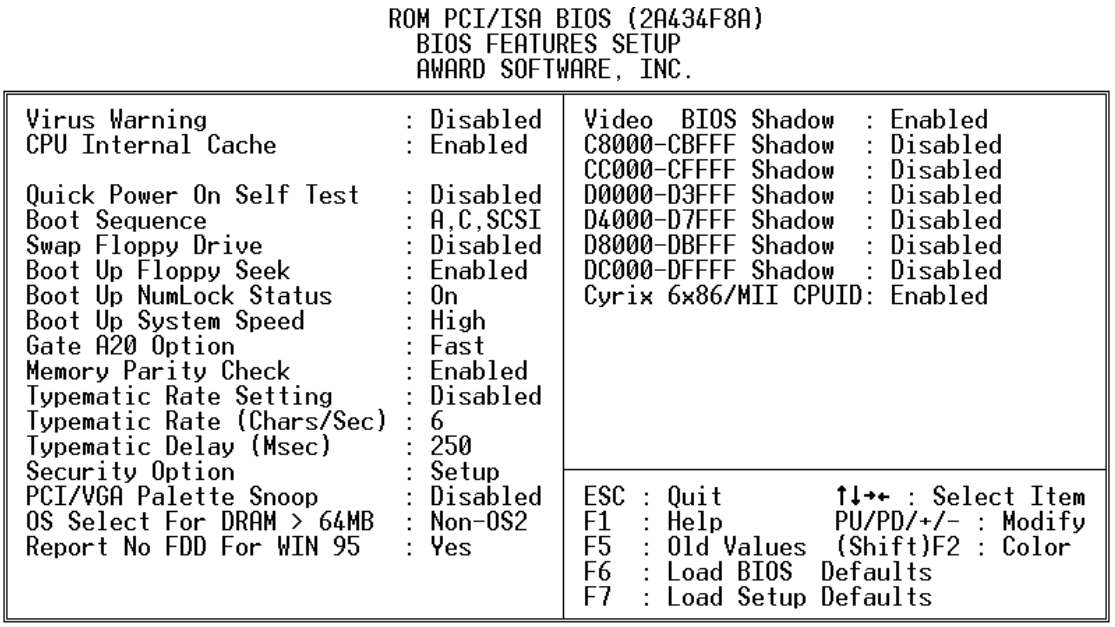
The BIOS determines how much extended memory is present during the POST. This is the amount of memory located 1MB in the CPU' s memory address map.

Other Memory

This item refers to the memory located in the 640K to 1024K address space. This is the memory that can be used for different applications. DOS uses this area to load device drivers in an effort to keep as much base memory free for application programs. The BIOS is the most frequent user of this RAM area since this is where it shadows RAM

4.3 BIOS Features Setup

This section allows you to configure your system for basic operation. You have the opportunity to select the system' s default speed, boot-up sequence, keyboard operation, shadowing and security. It allows you to improve your system performance, or let you set up according to your preference.



BIOS Features Setup

A section at the lower right of the screen displays the control keys you can use. Take note of these keys and their respective uses. If you need information on a particular entry, highlight it and then press<F1>. A pop-up help menu will appear to provide you with the information you need. <F5> loads the BIOS default values and Setup default values, respectively.

Virus Warning (Disabled)

When this item is enabled, the BIOS will monitor the boot sector and partition table of the hard disk for any attempt at modification. If an attempt is made, the BIOS will halt the system and the following message will display. If this occurs, you can either allow the operation to continue or use a bootable anti-virus floppy disk to restart and investigate the system.

! WARNING !
Disk boot sector is to be modified
Type " Y" to accept write or " N" abort write
Award Software, Inc.

Enabled	Activate a warning message and halt the system at the same time automatically when any activity attempts to access the boot sector or hard disk partition table.
Disabled	No warning message and system halt will appear when any activity attempts to access the boot sector or hard disk partition table.

Note:

Many disk diagnostic programs or operating system installations, which at-tempting to access the boot sector table can cause the above warning message. If you will be running such a program, we recommend that you first disable Virus Warning beforehand.

CPU Internal Cache

These two categories allow you to enable or disable the CPU Internal (Level 1).

Enabled	Enable cache
Disabled	Disable cache

Quick Power On Self Test (Disabled)

This category speeds up Power On Self Test (POST) routine by skipping retesting a second, third, and fourth time after you power up the SBC. Setup default setting for this field is enabled. A complete test of the system is done on each test. If this field is Enable, BIOS will shorten or skip some check items during POST.

Enabled	Enabled quick POST
Disabled	Normal POST

Boot Sequence (A, C, SCSI)

This category determines where the system looks first for an operating system (i.e., DOS). Options are A, C; A, CDROM, C; CDROM, C, A; E, A; F, A; C only; LS/ZIP, C; LAN, A, C; LAN, C, A; and C, A. The default setting is to check first the floppy disk and then the hard disk drive.

C, A	System will search for hard disk drive first, and then floppy disk drive.
A, C	System will search for floppy drive first, and then hard disk drive.
CDROM, C, A	System will search for CDROM drive first, then hard disk drive, and finally floppy disk drive.
C, CDROM, A	System will search for hard disk drive first, then CDROM drive, and finally floppy disk drive.

Swap Floppy Drive (Disabled)

This item allows you to switch between the floppy letter assignments without hardware modification.

The choice: Enabled/Disabled.

Boot Up Floppy Seek (Enabled)

During POST, BIOS will determine if the floppy disk drive installed is 40 or 80 tracks. 360K type is 40 tracks while 760K, 1.2M and 1.44M are all 80 tracks.

Enabled	BIOS searches for floppy disk drive to determine if it is 40 or 80 tracks. Note that BIOS can not tell from 720K, 1.2M. or 1.44M drive types as they are all 80 tracks.
Disabled	BIOS will not search for the type of floppy disk drive by track number. Note that there will not be any warning message if the drive installed is 360K.

Boot Up NumLock Status (On)

This allows you to determine the default status of the numeric keypad. By default, the System boots with NumLock on.

On	Keypad is number keys
Off	Keypad is arrow keys

Boot Up System Speed (High)

This allows you to determine the system speed when the system boots up. By default, the system boots up at high speed.

Gate A20 Option (Normal)

This entry allows you to select how the gate A20 is handled. The gate A20 is a device used to address memory above 1M bytes. Initially, the gate A20 was handled via a pin on the keyboard. Today, while keyboards still provide this support, it is more common, and much faster, for the system chipset to provide support for gate A20.

Normal	keyboard
Fast	chipset

Typematic Rate Setting (Disabled)

When disabled, continually holding down a key on the keyboard will generate only one keystroke. On the contrary, the BIOS will report repeated keystrokes when this field is enabled. For example, you may use this feature to accelerate cursor movements with the arrow keys.

Enable	Enable typematic rate
Disable	Disable typematic rate

Typematic Rate (Chars/Sec) (6)

This field controls the speed at which the system registers repeated keystrokes. When the typematic rate is enabled, this field allows you to select the keystroke rate. Options range from 6 to 30 characters per second. Setup default setting is 6; other settings are 8, 10, 12, 15, 20, 24 and 30.

6	6 characters per second
8	8 characters per second
10	10 characters per second
12	12 characters per second
15	15 characters per second
20	20 characters per second
24	24 characters per second
30	30 characters per second

Typematic Delay (Msec) (250)

This field sets the time interval for displaying the first and second characters. When the typematic rate is enable, this selection allows you to control the delay interval for displaying the first and second characters Four delay rate options are available: 250,5 00, 750 and 1000.

250	250 m second
500	500 m second
750	750 m second
1000	1000 m second

Security Option (Setup)

When you specify a Supervisor Password and/or User Password (explained later in this section), this option determines when the system prompts for password. It allows you to limit access to the system and Setup, or just to Setup. The default setting is Setup, where the system goes through its start-up routine unless the Setup utility is called, when the system prompts for the Supervisor Password.

System	The system will prompt for the User Password every time you start the system.
Setup	The system will prompt for the Supervisor Password only when the BIOS Setup is called.

Note:

To disable security, select "PASSWORD SETTING" at BIOS Setup "Main Menu" and then just type nothing but press <Enter> for the password. Once the security is disabled, you can boot the system and enter the Setup freely.

PCI / VGA Palette Snoop (Disabled)

This option determines whether the MPEG ISA/VESA VGA Cards can work with PCI/VGA or not. Some display cards that are non-standard VGA, such as graphic accelerators or MPEG video cards, may not show colors properly. "Enable" setting corrects this problem. Otherwise, leave this on the default setting of Disabled.

Enable	When PCI/VGA working with MPEG ISA / VESA VGA card.
Disable	When PCI / VGA not working with MPEG ISA / VESA VGA card.

Assign IRQ for VGA (Disabled)

The default value is Disabled.

Enable	Assign a specific IRQ for VGA
Disable	No IRQ is assigned for VGA

OS Select for DRAM > 64 (Non-OS2)

This item allows you to access the memory that over 64MB in OS/2. The choice: Non-OS2, OS2. The default setting is Non-OS2.

Report No FDD For Win95 (No)

This item allows Windows 95 to share IRQ6, which is assigned to a floppy disk drive, with other peripherals as if the floppy drive is not existing.

Video BIOS Shadow (Enabled)

This item allows the system to locate video BIOS from ROM to RAM for better video performance. However, it is an optional feature depending on the chipset and video BIOS design.

Enabled	Video shadow is enabled
Disabled	Video shadow is disabled

C8000-CBFFF Shadow to DC000 - DFFFF Shadow (Disabled)

These categories allow the system to shadow the ROMs of optional expansion controllers to RAM. To enable this feature, a specific shadowing address is necessary. An example of such ROM shadowing would be the support of onboard SCSI.

Enabled	Optional shadow is enabled
Disabled	Optional shadow is disabled

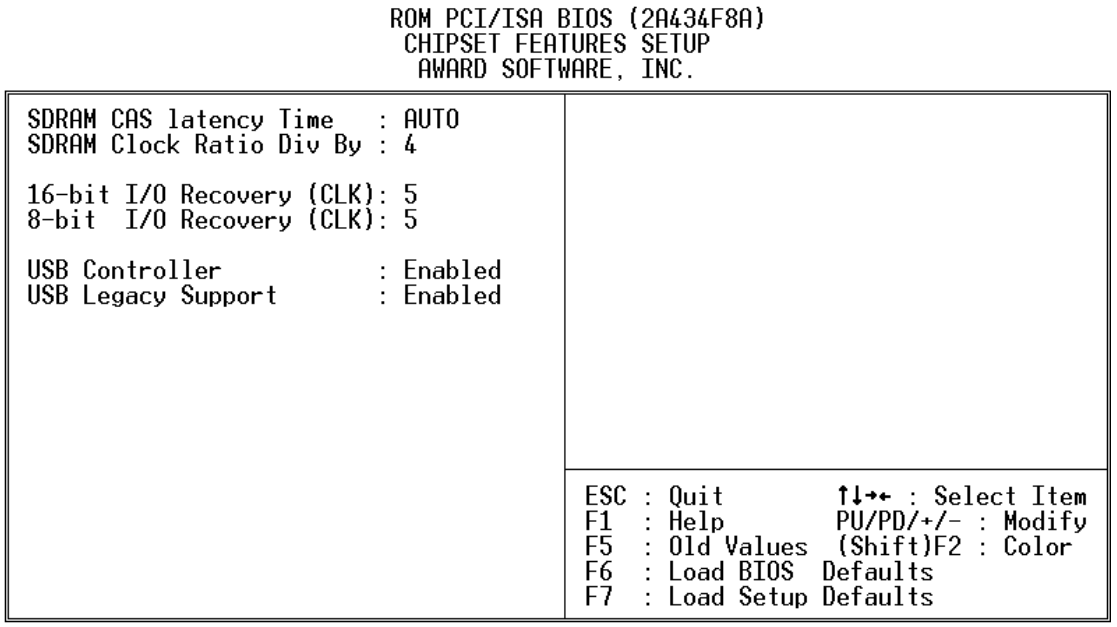
Cyrix 6x86/MII CPUID (Enabled).

4.4 Chipset Features Setup

This section and next section describe features of the NS Geode CS5530A Chipset. Chipset Features Setup controls the configuration of the SBC's chipset. Control keys for this screen are the same as in the BIOS Features Setup screen. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system.

Warning:

The parameters in this screen are for system designers, service personnel, and technically competent users only. Do not reset these values unless you understand the consequences of your changes.



Chipset Features Setup

SDRAM CAS Latency Time (3)

This field controls the CAS latency time in HCLK of 2/2 or 3/3. The value in this field is set according to the DRAM installed. Do not change the value in this field unless you change specification of the installed DRAM or CPU.

The Choice: 2, 3.

16-Bit I/O Recovery Time

8-Bit I/O Recovery Time

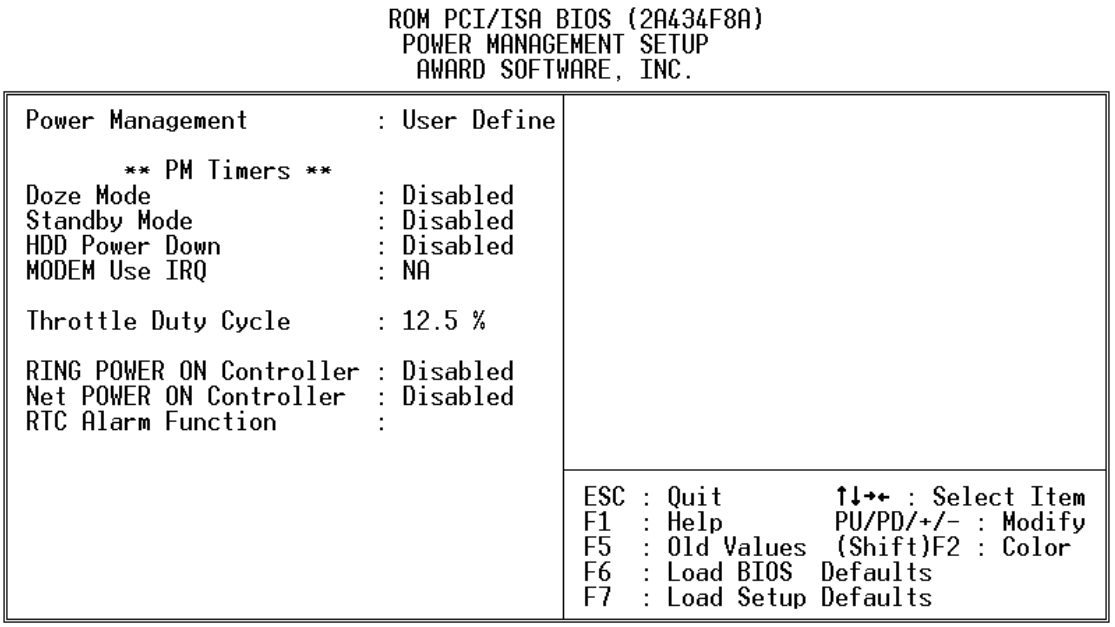
These options specify the length of the delay (in BUSCLK) inserted between consecutive 8-bit/16-bit I/O operations.

USB Controller (Disabled)

If you do not use the onboard USB feature, it allows you to disable it.
The options are: Enabled, Disabled (Default).

4.5 Power Management Setup

Power Management Setup allows you to reduce power consumption. This feature turns off the video display and shuts down the hard disk after a period of inactivity.



Power Management Setup

Power Management (User Define)

This category allows you to select the type (or degree) of power saving and is directly related to the following modes: Doze Mode, Standby Mode, Suspend Mode, HDD Power Down. There are three selections for Power Management

Min. Power Saving	Minimum power management. Doze Mode = 1 hr. Standby Mode = 1hr., Suspend Mode = 1hr., and HDD Power Down = 15min.
Max. Power Saving	Maximum power management – **ONLY AVAILABLE FOR SL CPUs.** Doze Mode = 1 min., Standby Mode = 1 min., Suspend Mode = 1 min., and HDD Power Down = 1 min.
User Defined	Allow you to set each mode individually. When not disabled, each of the ranges is from 1 min. to 1 hr. except for HDD Power Down, which ranges from 1 min to 15 min. and disable.

Doze Mode (Disabled)

When disabled, the system will not enter Doze mode. The specified time option defines the idle time the system takes before it enters Doze mode. The options are: Disabled (Default), 1, 2, 4, 8, 12, 20, 30, 40 Min, 1 Hr.

Standby Mode (Disable)

When this option is enabled and the setting time of system inactivity is due, the fixed disk drive and the video would be shut off while all other devices still operate at full speed.

HDD Power Down (Disabled)

The option lets the BIOS turn the HDD motor off when system is in Suspend mode. Selecting 1 Min.15 Min allows you define the HDD idle time before the HDD enters the Power Saving Mode. The options 1 Min., 15 Min will not work concurrently. When HDD is in the Power Saving Mode, any access to the HDD will wake the HDD up.
The options are: Disable (Default), 1 Min., 15 Min.

MODEM Use IRQ (NA)

This feature allows you to select the IRQ# to meet your modem' s IRQ#.
The options are: NA (Default), 3, 4, 5, 7, 9, 10, and 11.

Throttle Duty Cycle (12.5%)

When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of time that the clock runs.
The Choices: 12.5%, 25.0%, 37.5%, 50.0%, 62.5%, and 75.0%

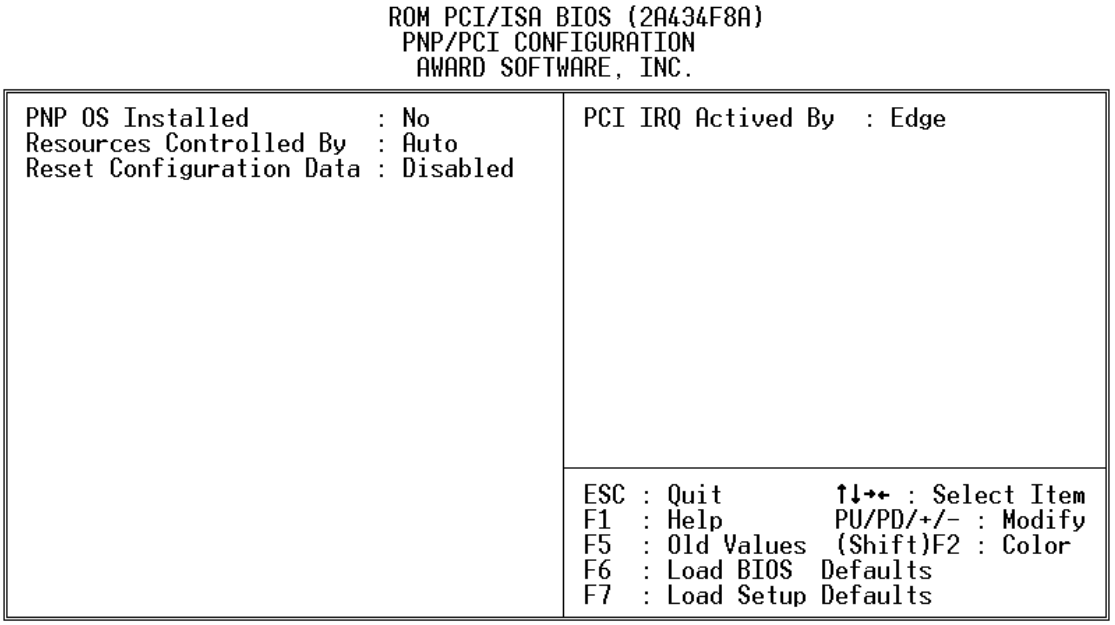
Ring Power On LAN Control (Disabled)

Net Power On Controller (Disabled)

RTC Alarm Controller (Disabled)

4.6 PnP/PCI Configuration

This section describes configuring the PCI bus system. PCI, or Personal Computer Interconnect, is a system, which allows I/O devices to operate at speeds nearing the speed the CPU itself, uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.



PnP/PCI Configuration

PnP OS Installed (No)

This field allows you to use a Plug-and-Play (PnP) operating system to configure the PCI bus slots instead of using the BIOS.

The Choice: Yes and No.

Resource Controlled by (Auto)

The Plug-and-Play BIOS can automatically configure all the boot and Plug-and-Play compatible devices. If you select "Auto", all the interrupt request (IRQ) and DMA assignment fields disappear, when the BIOS automatically arrange the assignments.

The Choice: Auto and Manual.

Reset Configuration Data (Disabled)

Normally, you leave this field "Disabled". Select "Enabled" to reset the Configuration Data, when you have installed a new add-on and the system has participated a serious configuration conflict, which causes the operating system to not boot.

The Choice: Enabled and Disabled.

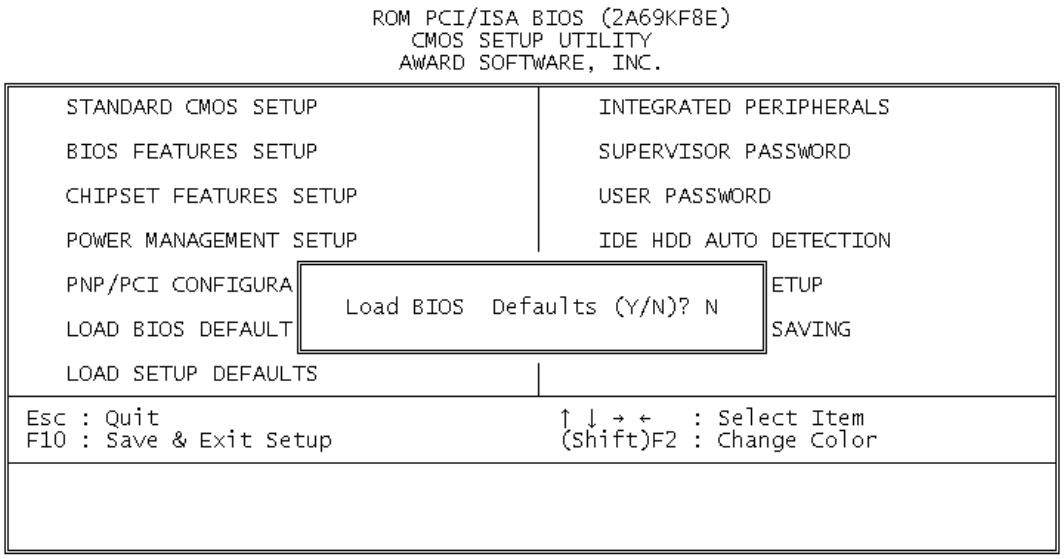
PCI IRQ Actived By (Level)

We suggest that you set this to its default configuration unless you are a qualified technician. The options are: Level (Default), Edge.

4.7 Load BIOS Defaults

This item allows the system to load back the "troubleshooting default values" stored permanently in the BIOS ROM. These BIOS defaults are designed to provide the minimum requirements for the system to operate.

To load the "BIOS defaults", highlight "Load BIOS Defaults" on the main menu and then press <Enter>. The system displays a confirmation message on the screen. Press <Y> and then <Enter> to load BIOS defaults. Press <N> and then <Enter> to abort.

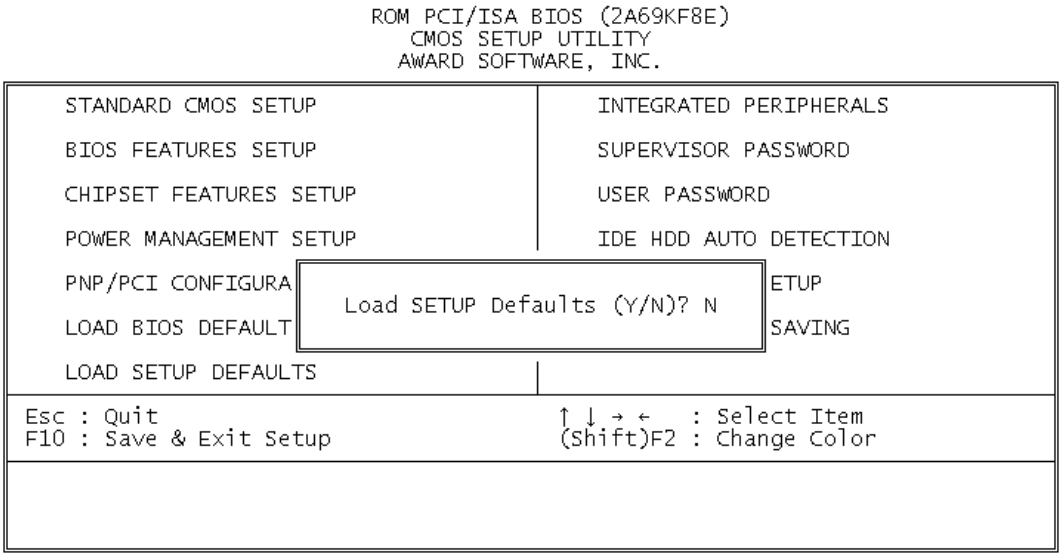


Load BIOS Default

4.8 Load Setup Defaults

This item allows the system to load back the "Setup defaults" which is designed to provide maximum system performance.

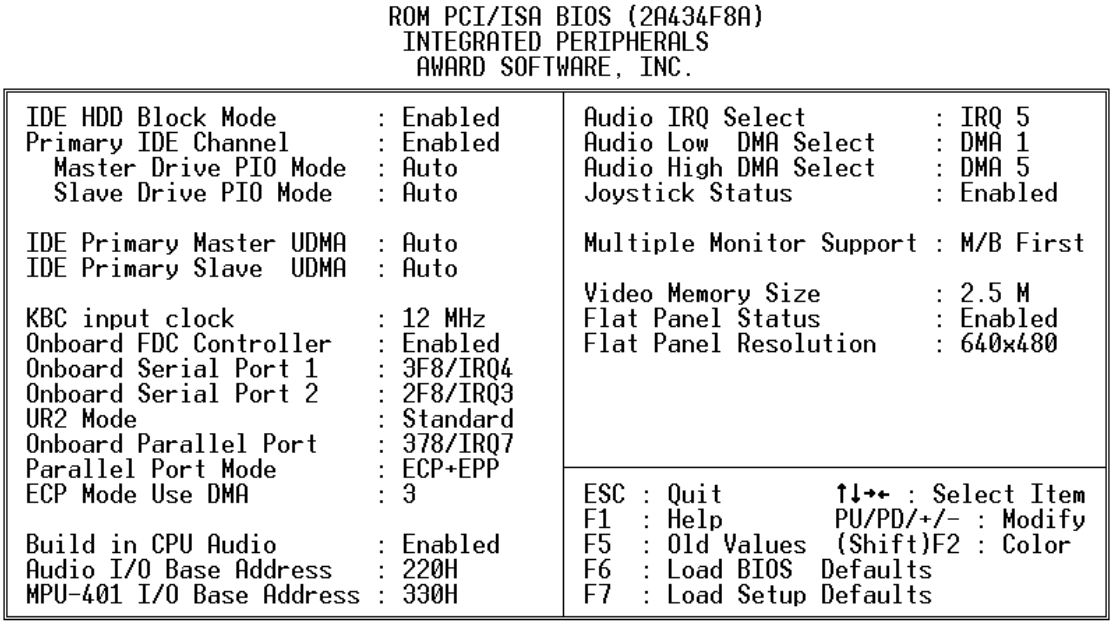
To load the "Setup defaults", highlight "Load Setup Defaults" on the main menu and then press <Enter>. The system displays a confirmation message on the screen. Press <Y> and then <Enter> to load Setup defaults. Press <N> and then <Enter> to abort.



Load Setup Default

4.9 Integrated Peripherals Features Setup

The parameters in this screen are for system designers, service personnel, and technically competent users only. Do not reset these values unless you understand the consequences of your changes.



Integrated Peripherals Features Setup

IDE HDD Block Mode (Disabled)

This allows your hard disk controller to use the fast block mode to transfer data to and from your hard disk drive (HDD).

Enabled	IDE controller uses block mode.
Disabled	IDE controller uses standard mode.

Primary IDE Channel (Enabled)

The integrated peripheral controller contains an IDE interface with support for IDE channel. Select Enabled to activate this channel.

Master / Slave Drive PIO Mode (Auto)

These four fields allow you to set PIO mode for each IDE device according to their different mode timing. Modes 0 through 4 provide successively increased performance. Choosing "Auto" mode will enable auto-detection to ensure optimal performance.

IDE Master/Slave Ultra DMA (Disabled)

Ultra DMA/33 implementation is possible, only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support UltraDMA/33, select Auto to enable Ultra DMA capability.

The Choice: Auto, Disabled

Keyboard Input Clock (8 MHz)

This item allows you to determine which input clock of your keyboard.

The Choice: 6MHz, 8MHz, 12MHz, 16MHz.

Onboard FDC Controller (Enabled)

When enabled, this field allows you to use the on-board floppy disk drive connector instead of a separate controller card. Set this field to "Disabled" if you want to use a separate controller card to connect the floppy disk drives.

The Choice: Enabled, Disabled.

Onboard Serial Port 1 (3F8/IRQ4) / Port 2 (2F8/IRQ3)

These items allow you to determine I/O addresses and IRQ lines for the on-board serial connectors.

The Choice: 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2F8/IRQ3, Disabled, Auto.

UR2 Mode (Standard)

This item allows you to activate the on-board infrared feature on COM2 connector. Choose "ASKIR" or "IrDA" according to the different Infrared device installed. Choose "Normal" to leave COM2 for general serial port UART support.

The Choice: Standard, Sharp IR, IrDA SIR, Midi.

Onboard Parallel Port (378/IRQ7)

This item sets the I/O address and IRQ line for the on-board parallel port connector. You can install an I/O card to support extra parallel port, if there is no conflict in the address assignments.

The Choice: 378H/IRQ7, 278H/IRQ5, 3BCH/IRQ7, Disabled.

Parallel Port Mode (ECP+EPP)

Allow you to connect with an advanced printer. Select SPP for standard parallel port (SPP) used on IBM PC/XT, PC/AT and bi-directional parallel port found on PS/2 system.

- Select EPP / SPP mode for enhanced parallel port and the standard parallel port.
- Select ECP mode for Microsoft and HP Extended Capabilities Parallel Port.
- Select ECP/EPP mode for both ECP and EPP modes.

The Choice: SPP, ECP+EPP1.7, EPP1.7+SPP, EPP1.9+SPP, ECP, ECP+EPP1.9, and Normal.

Multiple Monitor Support (M/B First)

This item allows you to determine which display mode of VGA adapter.
The Choice: M/B First, PCI First, No onboard

Flat Panel Resolution

Caution:
The BIOS setup for integrated peripherals, it is supported flat panel resolution either 640x480 or 800x600 mode at DOS mode.

4.10 Supervisor/User Password Setting

You can set either supervisor or user password, or both of then. The differences between are:

Supervisor Password: can enter and change the options of the setup menus.

User Password: just can only enter but do not have the right to change the options of the setup menus.

When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD:

Type the password, up to eight alphanumeric characters in length and with case sensitivity, then press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the sys-tem will boot and you can enter Setup freely.

PASSWORD DISABLED.

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorised person from changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorised use of your computer.

You can determine when the system should prompt for a password by adjusting the "Security Option" in "3-7 BIOS Features Setup. If the "Security Option" is set to "System", the password will be required both at "boot" and at "entry to Setup". If this is adjusted to "Setup", "Password Prompt" only occurs

when user tries to enter Setup utility.

4.11 IDE HDD Auto Detection

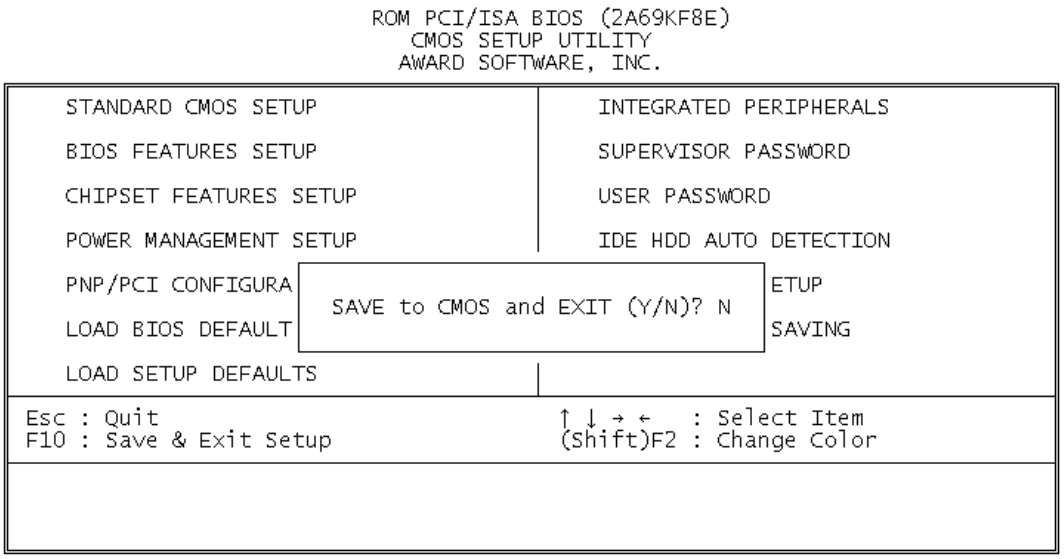
Automatically detect and configure hard disk parameters. The Award BIOS includes this ability in the event you are uncertain of your hard disk' s parameters. To accept the optimal entries, press <Y> or else select from the numbers displayed under the OPTIONS field; to skip to the next drive, press <N>. If you accept the values, the parameters will appear list beside the drive letter on the screen. The process then proceeds to the next drive letter. Pressing <N> to skip rather than to accept a set of parameters causes the program to enter zeros after that drive letter. When auto-detection is completed, the program automatically enters all entries you accepted on the field for that drive in the Standard CMOS Setup screen. Skipped entries are ignored and are not entered in the screen. Please also see, " Standard CMOS Setup" .

If your hard disk was already formatted on an older previous system, incorrect parameters may be detected. If the parameters listed differ from the ones used when the disk was formatted, the disk will not be readable. If the auto-detected parameters do not match the ones that should be used for your disk, do not accept them. Press <N> to reject the presented settings and enter the correct ones manually from the Standard CMOS Setup screen.

4.12 Save & Exit Setup

Save CMOS value changes to CMOS and exit setup. To save the configuration changes, highlight the "Save & Exit Setup" option on the main menu, type "Y", and then press <Enter>.

When you confirm the entries, and save them, the system will automatically reboot, and per-form the changes you made.



Save & Exit Setup

4.13 Exit Without Save

Abandon all CMOS value changes and exit setup. To exit without saving, highlight the "Exit Without Saving" option on the main menu and then press <Enter>. BIOS CMOS will retain the original setting.

4.14 Flash BIOS Writer Utility

Use AWDFLASH.EXE file in the "FIC SBC Driver & Utility CD for MBM-530NS" to update your system BIOS. Please follow the procedure below to backup and update your system BIOS.

4.14.1 Backup BIOS to file

1. Create a bootable system floppy diskette by typing "format a:/s" from the DOS Prompt, and then copy AWDFLASH.EXE to this diskette.
2. Re-boot the system and run AWDFLASH.EXE from this diskette, your screen will show the table below.
3. Press <Enter> for the "File Name to Program:" window.
4. Enter "Y" to the "Error Message: Do You Want To Save Bios (Y/N)"
5. Enter the "Current BIOS Revision" as the file name into the "File Name to Save:" window, and then press <Enter>. The file name could be in the format of "REVISION.BIN" for easy identification. For example, 2A434F8A.BIN.
6. Store this "BIOS Backup Diskette" in a safe place for future use.

4.14.2 Update BIOS from file

1. Make a "BIOS Backup Diskette" as shown above before you start step 2.
2. Create another bootable system floppy diskette by typing "format a:/s" from the DOS prompt, and then copy AWDFLASH.EXE to this "BIOS Update Diskette".
3. Copy the new BIOS file to this "BIOS Update Diskette".
4. Re-boot the system and run AWDFLASH.EXE from "BIOS Update Diskette", your screen will show the table below.
5. 5. Enter the new BIOS file name with extension into the "File Name to Program:" window, and then press <Enter>.
6. Enter "N" for the "Error Message: Do You Want To Save Bios (Y/N)"
7. Enter "Y" to the "Error Message: Are you sure to program (y/n)". The Flash Memory Writer will now renew the BIOS from disk file.
8. After successfully updating the new BIOS file, a message similar to "Programming Flash Memory – 1FF00 ok" will be shown on the screen.
9. Take the "BIOS Update Diskette" out of floppy drive and then re-boot your system.
10. You may hold down <Delete> to adjust the new BIOS setup now.

5. SPECIFICATION

5x86 All–in-one Multimedia Embedded Computer with VGA/LCD/LAN CPU.

* **CPU**: NS GX1-300 Lower Power CPU.

* **Chipset**: Geode CS5530A.

* **RAM Memory**: one 144-pin SODIMM Socket Supports up to 256MB SDRAM.

* **L2 Cache Size**: None.

* **Flash Disk**: Provides One Socket for 2MB-288MB DiskOnChip.

* **PCI IDE**: Supports PIO MODE 4 IDE Devices 44-pin 2.00mm header for DOM/HDD.

* **Super I/O**: PC97317 Super IO Chipset.

  FDD Port – Supports 3.5" or 5.25" Floppy Devices

  Parallel Port –Supports SPP/EPP/ECP Mode

  COM Port – One RS232C, One RS232C/RS485C with 5V /12V Selected by Jumper

  IR Port – One 115Kbps IrDA Compliant Serial Infrared

* **TTL I/O**: Two TTL level input / Two TTL level output

* **Ethernet**: Support Realtek 8139C 10/100M Base-T Ethernet with RJ45-LED indicator Connectors.

* **USB**: Supports Two USB Ports.

* **KB + Mouse**: PS/2 Keyboard and Mouse with On board connector.

* **BIOS**: Award BIOS (256KB, including VGA BIOS).

* **Real Time Clock**: Built-in RTC with Backup Battery

* **Power Management**:

  Supports I/O Peripherals Power Saving / Doze / Standby / Suspend Modes satisfying APM1.2 Compliant.

* **Sound**: LM 4548 Audio Chipset Supports Mic_in/Line_in/Line_out Functions.

* **Display**: Geode CS5530A is Built-in with VGA/LCD Display Function Sharing with System Memory 4MB.

  Supports CRT Display Resolution 1024X768 @64K Colors(max) and 18 Bit TFT LCD Display Simultaneous.

  Supports LCD Back Light Control Connector

* **LED Indicators**: Power LED and IDE LED

* **EXT BUS**: 16 Bit PC/104 BUS and 32 Bit PCI BUS (PCI Bus depends on the PCB Size).

* **WDT**: Programmable WDT Providing 2-32 sec Timer Intervals with LED indicator.

* **Power Req.**: +5V/2A and 12V/0.5A (Max)

* **CE Design-In**: Add EMI Components to COM ports, Parallel Port, Keyboard, and PS/2 Mouse.

* **PC Board**: 6 layers.

* **Dimensions**: PC/104 Bus and PCI Slot, 140mm x 145mm

6. PROGRAMMING RS-485

The majority of the communicative operations of the RS-485 are the same as the RS-232. When the RS-485 proceeds with transmission, which needs control the TXC signal (RS-232 and RS-485 control the signal differently), the installation steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

Note:

Please refer to the "Serial Port" section in the chapter "System Controller" for the detailed description of the COM port's register.

(1) Initialize COM port

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets at "0".

NOTE: This is to control the MBM-530NS CPU card's DTR signal to the RS-485's TXC communication.

(2) Send out one character (Transmit)

Step 1: Enable the TXC signal, and the bit 0 of the address of offset+4 just sets at "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data to empty. Check the transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) is all sets that must be at "0".

Step 4: Disabled the TXC signal, and the bit 0 of the address of offset+4 sets at "0"

(3) Send out one block data (Transmit – the data more than two characters)

Step 1: Enable the TXC signal, and the bit 0 of the address of offset+4 just sets at "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data to empty. Check the transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) is all sets that must be at "0".

Step 4: Disabled the TXC signal, and the bit 0 of the address of offset+4 sets at "0".

(4) Receive data

The RS-485's operation of receiving data is the same as the RS-232's.

(5) Basic Language Example

a.) Initial 86C450 UART

```
10  OPEN "COM1:9600,m,8,1" AS #1 LEN=1
20  REM Reset DTR
30  OUT &H3FC, (INP(%H3FC) AND &HFA)
40  RETURN
```

b.) Send out one character to COM2

```
10  REM Enable transmitter by setting DTR ON
20  OUT &H3FC, (INP(&H3FC) OR &H01)
30  REM Send out one character
40  PRINT #1, OUTCHR$
50  REM Check transmitter holding register and shift register
60  IF ((INP(&H3FD) AND &H60) >0) THEN 60
70  REM Disable transmitter by resetting DTR
80  OUT &H3FC, (INP(&H3FC) AND &HEF)
90  RETURN
```

c.) Receive one character from COM2

```
10  REM Check COM2: receiver buffer
20  IF LOF(1)<256 THEN 70
30  REM Receiver buffer is empty
40  INPSTR$"
50  RETURN
60  REM Read one character from COM2: buffer
70  INPSTR$=INPUT$(1,#1)
80  RETURN
```

7. SUPPORT FACILITATION

This chapter gives the details of how to use the pre-programmed Watchdog Timer to monitor the industrial Automation system and provides the information on the included software.

WDT Time Table

GPIO / Step	1	2	3	Time Period (sec)
0	0	0	0	2
1	0	0	1	4
2	0	1	0	8
3	0	1	1	16
4	1	0	0	20
5	1	0	1	24
6	1	1	0	28
7	1	1	1	32

WDT I/O Port

443H	I/O Write	The enable cycle
443H	I/O Write	The refresh cycle
441H	I/O Write	The disable cycle

Sample Program

```
#include <stdio.h>
#include <stdlib.h>
#include <dos.h>

#define Count01  0x01       //GPIO10
#define Count02 0x02        //GPIO11
#define Count03 0x04        //GPIO12
#define WDT_EN_IO  0x443     //IO for Enable WDT
#define WDT_DIS_IO0x441     //IO for Disable WDT

unsigned    Index_Reg = 0x002E, Data_Reg = 0x002F;
unsigned char Dev_Index = 0x07, GPIO_Num = 0x07, PM_Num = 0x08;
```

```
void main(int argc, char* argv[]) {
  int i,count;
  int setting[8]={2,4,8,16,20,24,28,32};
  unsigned char
mBAR,lBAR,PM_Index_Reg,PM_Data_Reg,GPIO_En,port_Select,CFG
DAT;
  unsigned PMBAR,GPIOBAR;

  if ((argc<2)||(atoi(argv[1])<1)) count=2;      //Default setting
  else count= (int)(atoi(argv[1]));
  for(i=0; i<8; i++) {
    if (count == setting[i]) break;
   }
  if (i==8) {
    printf("WDT530  [count] (count = 2, 4, 8, 16, 20, 24, 28, 32)\n");
      exit(-1);
   }

  outportb(Index_Reg, Dev_Index);      //Choose Logical Dev. PM
  outportb(Data_Reg, PM_Num);          //
  outportb(Index_Reg, 0x30);         //Enable PM register access
  outportb(Data_Reg, 0x01);          //
  outportb(Index_Reg, 0x60);         //PM Base address MSB
  mBAR = inportb(Data_Reg);          //
   outportb(Index_Reg, 0x61);        //PM Base address LSB
  lBAR = inportb(Data_Reg);          //
  PMBAR = ((unsigned)mBAR <<8) + ((unsigned)lBAR);
  PM_Index_Reg = inportb(PMBAR + 0x00);      //GPIO ports function
enable
  PM_Data_Reg = inportb(PMBAR + 0x01); //
  outportb(PM_Index_Reg, 0x01);        //
  GPIO_En = inportb(PM_Data_Reg);  //
  outportb(PM_Index_Reg, 0x01);        //
  outportb(PM_Data_Reg, (GPIO_En | 0x80));//

  outportb(Index_Reg, Dev_Index);      //Choose Logical Dev. GPIO
```

```
    outportb(Data_Reg, GPIO_Num);            //
    outportb(Index_Reg, 0x30);       //Enable GPIO register access
    outportb(Data_Reg, 0x01);        //
    outportb(Index_Reg, 0x22);       //GPIO Bank select
    port_Select = inportb(Data_Reg);//
    outportb(Index_Reg, 0x22);       //GPIO port1 select
    outportb(Data_Reg, (port_Select & 0x7F));      //
    outportb(Index_Reg, 0x60);       //GPIO Base address MSB
    mBAR = inportb(Data_Reg);        //
    outportb(Index_Reg, 0x61);       //GPIO Base address LSB
    lBAR = inportb(Data_Reg);        //
    GPIOBAR = ((unsigned)mBAR <<8) + ((unsigned)lBAR);
    outportb((GPIOBAR + 0x01), 0x0f);    //set output direction

    CFGDAT=i;
    outportb(GPIOBAR,CFGDAT);          //Setting WDT count
    outportb(WDT_EN_IO,0xFF);          //Enable WDT

}
```